	FEDERAL UNIVERSITY OF TECHNOLOGY MINNA, NIGERIA
	SCHOOL OF ELECTRICAL ENGINEERING AND TECHNOLOGY
	DEPARTMENT OF MECHATRONICS ENGINEERING
	FIRST SEMESTER 2019/2020 ACADEMIC SESSION

MCE 316: Analogue Electronics

TIME ALLOWED: 2 HOURS	CREDIT UNIT: 2	LEVEL: 300

Instruction: Attempt 4 (four) Questions in all two from each of the section A and B.

Section A

Question 1 (25marks)

(a.) Draw a suitable op-amps circuit for each of the following sources, hence deduce an equation to suite their respective functions.

i.   Voltage Control voltage sources (VCVS)
ii.   Voltage Control Current sources (VCCS)
iii. Current Control voltage sources (CCVS)
iv.   Current Control Current sources (CCCS)

(b.) Calculate the output voltage for the circuit in figure 1 given the inputs voltage as
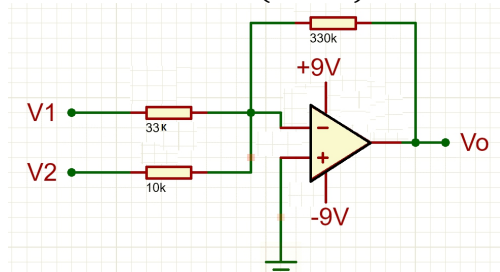$V1 = 50\ mV\ sin(1000t)\ and\ V2 = 10\ mV\ sin(3000t)$

figure 1

Question 2 (25marks)

(a.)   Explain the term Phase lock Loops (PLL) and list the unit that made-up the PLLs
(b.)   Enumerate (4) four advantages and (4) four disadvantages of the Phase lock loop Synthesizer
(c.)   i. Draw a block diagram of SE/NE 565 IC
   ii. Enumerate any 6(six) important electrical characteristics of the Monolithic Phase-Locked Loop (PLL) ICs

Question 3 (25marks)

(a.)   Differentiate between Analogue and Digital System with two example each.
(b.)   List (5) five advantages of digital system over its analogue counterpart
(c.)   Determine the output voltages caused by each bit in a 6-bit ladder if the input levels are 0 equals to 0V and 1 equal to +16V. Determine the resolution and full-scale output of this circuit. Find the output voltage from the above ladder for a digital input of 101011.

Section B

Question 4 (25marks)

(a) With respect to the circuit in **FigQ4**, the signal source is a variable
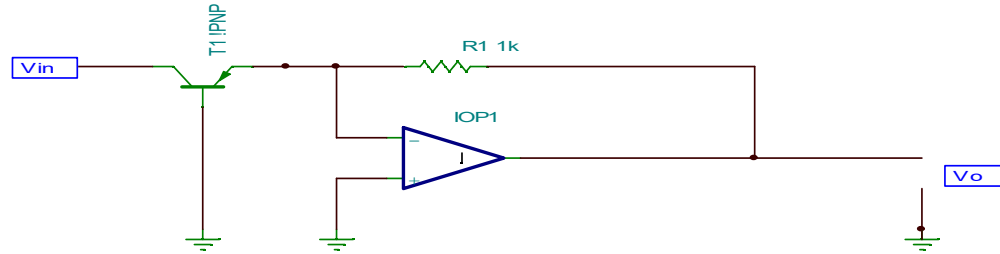
FigQ4

For the components $R_f = 60k\Omega$, $I_{EBO} = 50nA$, Determine Vo given the following Vin values: 175mV; 180mV; 185mV; 190mV; 195mV; 200mV respectively

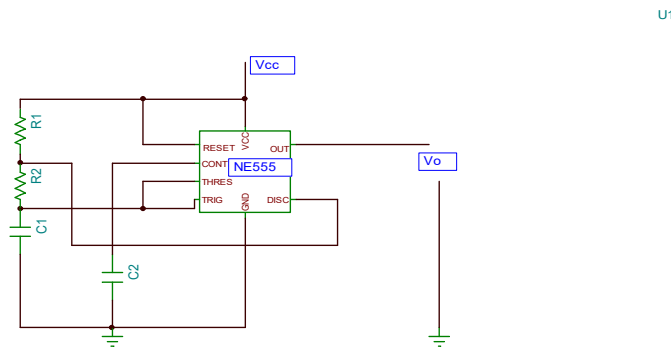(b) Name the circuit of **FigQ4** according to international standards

(c) What does the circuit of **FigQ4** accomplish in electronic systems?

(d) (i) Re-draw the circuit of **FigQ4** with an NPN transistor

  (ii) Re-draw the circuit of FigQ4 with any FET variant to replace the BJT

Question 5 (25marks

With reference to the circuit in **FigQ5** below;

FigQ5

  $V_{cc} = 6V$; R_1 = Interchangeable as specified under instruction ; $R_2 = 4.7$ kΩ ; $C_1 = 0.2$ pF ; $C_2 = 0.02$ µF respectively

  (a) (i) What mode is the 555 timer IC connected?

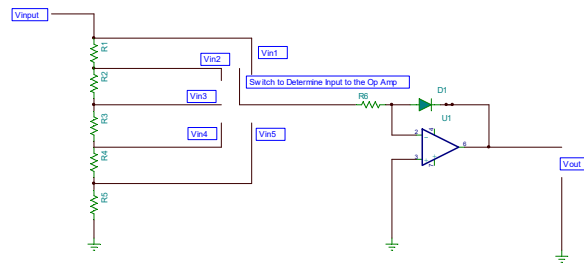   (ii) The frequency of the signal at the output with $R_1 = 2.2$ kΩ

    (iii) The frequency of the signal at the output with $R_1 = 10$ kΩ

    (iv) Duty cycle of the circuit in FigQ5 at $R_1 = 10$ kΩ

    (v) The waveform at the duty cycle value arrived at in (iv) above (that is, when $R_1 = 10$ kΩ)

  (b) Modify the circuit in FigQ5 into a tone generator

Question 6 (25marks

FigQ6

(a) Calculate voltage input to the amplifier at each point across each resistor (R_1 to R_5), and the corresponding output voltage from the amplifier given the peculiarities: $V_{in} = 5V$; $I_R = 50nA$; R_1 to $R_5 = 10k\Omega$, $R_6 = 20\ k\Omega$

    (i)   Calculate Vin_1 and the corresponding amplifier output voltage

    (ii)   Calculate Vin_2 and the corresponding amplifier output voltage

    (iii)   Calculate Vin_3 and the corresponding amplifier output voltage

    (iv)   Calculate Vin_4 and the corresponding amplifier output voltage

    (v)   Calculate Vin_5 and the corresponding amplifier output voltage

(b)(i) State the role of the resistors R1, R2, R3, R4, and R5 in the circuit of FigQ6 above

   (ii) Write the standard name of the amplifier in the circuit of FigQ6 above