# DESIGN AND CONSTRUCTION OF THREE- DIGIT (0 – 999) COUNTER

*BY*

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OCTOBER, 2006

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A Thesis Submitted to the Department of Electrical and Computer Engineering, Federal University of Technology, Minna, Niger State

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# DEDICATION

This project is dedicated to almighty God for his love, mercies and protection throughout my life and throughout my course of studies.

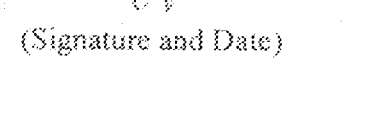
Also to my wonderful parent, Mr and Deaconess Ayodele for their love and support during the study.

# DECLARATION

I, **Ayodele A. James,** declare that this work was done by me and has never presented elsewhere for the award of a degree. I also hereby relinquish the copyright to the Federal University of Technoogy, Minna.

Ayodele A. James

(Student)



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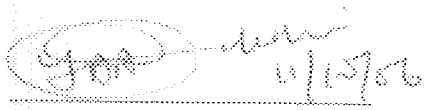

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(External Examiner)

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My sincere gratitude goes to the family of overseer and Dns Ogunwale, Mr and Mrs Adebisi, Dr and Mrs Olayemi, Mrs Balogun and Barr. and Dns Ayodele, who have been wonderful to me.

Finally, lots of thanks go to my friends: Olaleye Deji, Olofin Babajide, Oladumoye Ibilola, Grace, Glory, Junmoke, Asipa, Tunde, Daddy mike and Ojo Tosin. Also to others I can not mention. We are too strong to be defeated.

# ABSTRACT

This project reports the design and construction of three-digit (0 – 999) counter. The counter converts the square wave pulse signal applied to its input to the binary coded decimal (BCD) and which is, in turn, converted to digital decimal displays. These square wave pulses are generated manually by the press of a pushbutton. The pulses generated are applied to a cascade of decade counters and BCD to seven segment display driver. The number of pulses generated are counted, converted and then displayed in decimal form on three seven – segment displays, to form a three digit decimal display.

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# CHAPTER ONE

# INTRODUCTION

The design and construction of three – digit (0 – 999) counter aims at using the reliability and efficiency of the digital counter technology, which is being improved on by electronics engineer. The project aims to use this technology to improve on its versatility and adaptability.

Digital counter is an instrument which, in its simplest form, provides a numerical decimal display (output) that corresponds to the number of pulses applied to the input terminal.

Technically, digital counter is a device which connects flip-flops together to perform counting operation. The number of flip-flops connected and the manner in which they are connected determines the number of states called the modulus (MOD). The modulus also specifies the sequence of states that the counter goes through during each complete cycle.

Counters are categorized into two types according to the manner of the clock pulses applied to their inputs. They are categorized into synchronous and asynchronous counters. The asynchronous counter, often called the ripples counter, has the external clock pulse applied to the first flip-flop and successive flip-flops are clocked by the output of the preceding flip-flop. The binary counter obviously counts upward in standard binary code is called an up counter. It is also called an asynchronous counter. This is because the flip-flop do not change their state simultaneously. The second flip-flop

cannot change until the first flip-flop has already changed state. The third flip-flop can not change until the second flip-flop has charged an so on.

Flip-flops could be combined to make both asynchronous (ripples) and synchronous counter. In practice, using discrete flip-flops is to be avoided. Instead the use of a prefabricated integrated circuit (IC) counter is advised. These also come in either synchronous or asynchronous (ripple) form and are usually designed to count in binary or binary coded decimal (BCD).

The term asynchronous also refers to events that do not have a fixed time relationship with each other and generally do not occur at the same time. Therefore, asynchronous counter is the one which the flip-flop in the counter IC does not change at exactly the same time because they do not have common pulse.

The counter that we have seen so far is asynchronous. That is, each flip-flop must wait until the previous flip-flop has changed before the two can change. But a counter where all the flip-flops change at the same time is called synchronous counter. A counter designed so that all the counter outputs change at the same time is called synchronous counter. A counter designed so that all the counter outputs change at the same time called synchronous counter.

In synchronous counters, the clock pulse is applied to all the flip-flops at the same time, in a manner they are clocked simultaneously. The synchronous counter contains a cascade of flip-flops that are applied to same clock pulse at the same time and hence, does not accumulate nearly as many propagation delays as is the case with the asynchronous counter.

However, the asynchronous type of counter is used in this project. It operates in binary number system since binary is easily implemented with electronics circuitry and also it allows any integer (whole number) to be represented as a series of binary digits or bits where each but is either a zero (0) or one (1) that is, high or low. [1, 2, 3]

## 1.1 MODE OF OPERATION

The three – digit counter consist of a cascade of combinational circuits. The pulses are generated manually (manual mode).

When a power supply is switched on, the pulse wave from generator circuit will start to oscillate, the pulse being produced from the pulse generator circuit is fed with 7490 digital integrated circuit (IC) which is a decade counter.

The output from this 7490 digital integrated circuit is fed into 7448 decoder/driver integrated circuit (IC) where the signal from the 7490 IC decodes and passes into common cathode seven segment display. The number of pulses being produced from the pulse generator circuit is then displayed on the common cathode seven-segment display.

The circuiting is grouped into different units, namely: manual pulse generator circuit, decade counter, BCD decoder/drivers, seven segment display, power unit. The function of each section is stated below:

### 1.1.1 Manual Pulse Generator Circuit

This section generates square wave pulses by the action of presenting the push button.

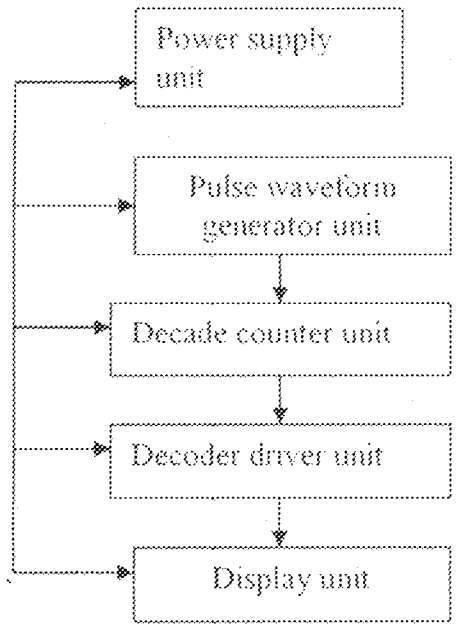



Fig 1.1: Block diagram of 0 – 999 three digit counter

## 1.2 MOTIVATION

Modern devices in a global term are getting more digitalized. The need for electronics digital display has increased and more devices are requiring the use of digital displays and counters. Almost all modern electronic equipment or devices are being digitally controlled and as well have digital numeric display, which are all made up of digital counter.

The display on digital radio receivers, television sets, electronic devices iterates the efficiency and convenience provided by the digital counters. The ease by which the digital counter can be adapted and its effectiveness prompt the idea for the three-digit counter. Most modern electronic equipment from laboratory equipment to kitchen hardware, are being controlled by digital counter technology. Modern electronic measuring instruments from hospital thermometer to digital volumeter also use digital display and counter. Digital counters are used in the control of traffic system, digital clock, electronics score board and bill boards. All these vast application and adaptability

of the digital counter attest to the effectiveness, efficiency and widespread use and acceptance of the digital counting technology; hence, the motivation to adopt the digital counting technology to achieve the purpose of this project work.

## 1.3 OBJECTIVES

1. To design and construct a simple low cost, low power device to aid the counting of an object manually.
2. To design end construct a device to aid the manual count of people in a gathering.
3. To ease the counting of objects.

# CHAPTER TWO

# LITERATURE REVIEW

The awareness of number has extended and vivid so that a need was felt to express the property in some ways, presumably at first in sign language only.

The finger on a hand can be readily used to indicate a set of one (1), two (2) three (3), four (4) or five (5) objects. The numbers are generally not recognized at first as true number.

By the use of fingers of both hands collection containing up to ten elements, could be represented. By combining fingers and toes, one could count as high as twenty (20). When the human digits were inadequate heaps of stones were used to represent a correspondence with the element of another set. Where non – literate people used such a scheme or representation, they often piled the stones in groups of five (5), for they had become familiar with quintuples through observations of the human hand and foot.

As Aristotle (father of philosophy) had noted long age, the undesired use today of the decimal system is, but a result of anatomical accident that most of us are born with ten fingers and then toes.

Groups of stones are ephemeral for presentation of information, hence, prehistoric man sometimes made a number recorded by cutting notches in a stick or a piece of bone. However, there are limitations in these tedious and manual ways of counting. As a result of short memory of man, these various activities of man led to the development of machine used in counting and storing.

It is called a counting machine. A counting machine could be in form of electrical counter or mechanical counter [4].

## 2.1 COUNTING MACHINE

Many fields of industry and commerce have to use counting devices of one sort or the other. The most familiar type is probably the distance recorder of cars, which is a simple type of mechanical counter. The same device is used in the hand held, used for example to record the number of people passing in a given point such as a station exit.

Counters in time prior to now took many forms which include geared machines used in tape recorder counter and distance recorder of cars, relays used in old pinball machines and telephone switching system. Counting machine could be either mechanical counter or electrical counter.

### 2.1.1 MECHANICAL COUNTERS

These work on the mechanism of a claw operation on a result ratchet wheel with ten teeth. Each back and forth movement of the claw pulls the wheel round one tooth. A wide ring with numerals round its rim is attached to the wheel and there is usually a casing with a window of the claw, thereby bringing the next numeral into view. There are usually several of these wheels side by side, each operated by the one on its right that moves on one number for every complete turn of the first. This automatically produces counting of tens, hundreds, thousands and son on.

### 2.1.2 ELECTRONIC COUNTER

Mechanical counters have the disadvantages of slow operation. They take a fraction of a second to change number that makes them unsuitable for high speed counting rates. In such cases, it is common to use electronics counter of one kind or the other [5].

Electronics counter can be defined as instrument which automatically counts and indicates the total of a succession of electrical pulse or of other repetitive phenomenon that can be converted into pulses. These electronics circuits have no mechanical inertia, so electronic counters attain higher speeds than the fastest electro-mechanical counter sometimes up to several million events per second. Consequently, these are useful in measuring radio wave frequency in laboratories or in counting pulses for electronic computer read out devices [6].

Counting operation is mostly implemented in binary from using number sequence or system, since these are easily implemented with electronics. Binary counter allows any integer to be represented as a series of binary digits or bits where each bit is either a zero (0) or one (1). And after being worked on by the necessary component like the ICs which are of different functions and various transistors and diodes, it displays out the appropriate decimal as its output [3].

## 2.2 THEORETICAL BACKGROUND

### 2.2.1 ASYNCHRONOUS COUNTERS

A counter is a special type of sequential circuit with a single clock input and a number of outputs. Each time the counter is clocked, one or more of the outputs

change state. These outputs from a sequence with N unique values. After the Nth value has been observed at the counter's output terminals, the next clock pulse causes the counter to sequence. That is, the sequence is cyclic. A counter composed of M flip-flops can generate an arbitrary sequence with a length of not greater than $2^m$ cycles before the sequence begins to repeat itself.

One of the tools frequently employed to illustrate the operation of sequential circuits is the state diagram. Any system with internal memory (e.g. flip-flops) and external inputs can be said to be in a state which is a function of internal and external inputs. A state diagram shows some (or all) of the possible state of a given system. Each of the state can be linked by unidirectional lines showing the path by which one state becomes another state.

The state diagram of a JK flip-flop has only two states, $S_1$ and $S_2$ as we can see from figure 2.1 $S_1$ represents the state Q = 0 and $S_2$ represent the state Q =1. Transitions between state are determined by the values of the JK inputs at the time the flip-flop is clocked. Table 2.1 defines the four possible input condition, $C_1$, $C_2$, $C_3$ and $C_4$, interview of J and K.

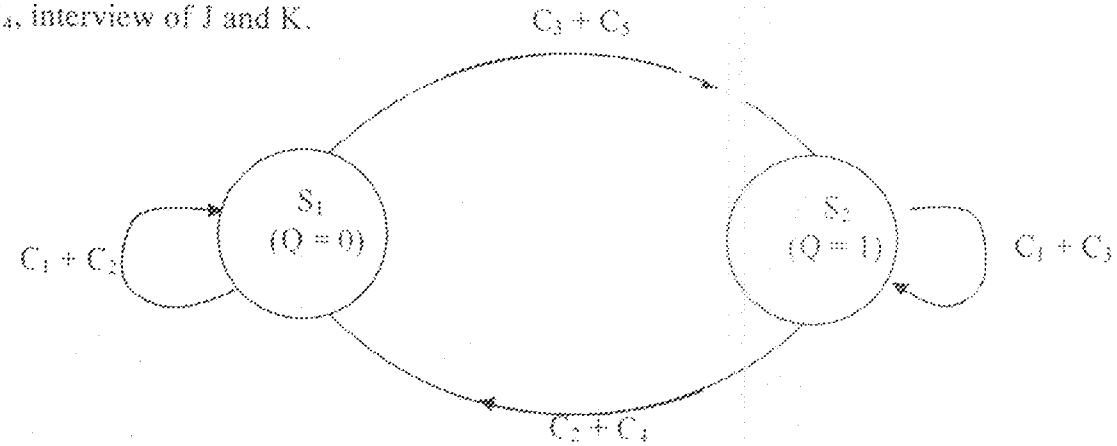



Fig 2.1: The State diagram of a JK flip-flop

Table 2.1: Relationship between J, K and condition $C_1 - C_4$

| J | K | Condition |
|---|---|---|
| 0 | 0 | $C_1$ |
| 0 | 1 | $C_2$ |
| 1 | 0 | $C_3$ |
| 1 | 1 | $C_4$ |

It can be seen that conditions $C_3$ or $C_4$ causes a transition from state $S_1$ to state $S_2$. Similarly, condition $C_2$ or $C_4$ cause a transition from $S_2$ to state $S_1$. Note that condition $C_4$ causes a change of state from $S_1$ to $S_2$ and also from $S_2$ to $S_1$, that is, of course, the condition J = K = 1 which causes the JK flip-flop to toggle its output. Note also that some condition causes a state to change to itself, that is, there is no overall change. Thus conditions $C_1$ and $C_2$, when applied to system in state $S_1$, have the effect of leaving the system in state $S_1$.

### 2.2.2 BINARY UP-COUNTER

The state diagram of a simple n – bit binary up-counter is given in figure 2.2. In this example, there is only a single path from one state to its neighbour. As the system is clocked, it cycles through the states $S_0$ to $S_n$, which represent the natural binary number 0 to n. The actual design of counters in general can be quite involved, although the basic principle is to ask; what input conditions are required by the flip-flops to cause them to change from state $S_i$ to state $S_{i+1}$?.

The design of an asynchronous natural binary up-counter is rather simpler than the general case (that is, of a counter of an arbitrary sequence). The JK inputs, to each flip-flop are connected to constant logical one level. Consequently, whenever flip-flops is clocked, its output changes state. The flip-flop are arranged so that the Q output of one device triggers the clock input of the next device. Hence, master slave.

The asynchronous counter of this form is also called a ripple counter because the output of the first state triggers the input of the second stage and the output of the second stage triggers the input of the third stage, and so on. Consequently a change of state at the output of the first stage ripples through the counter until it clocks the final stage. An n – bit binary counter composed of JK flip-flops is shown in figure 2.3. [1, 2, 7]

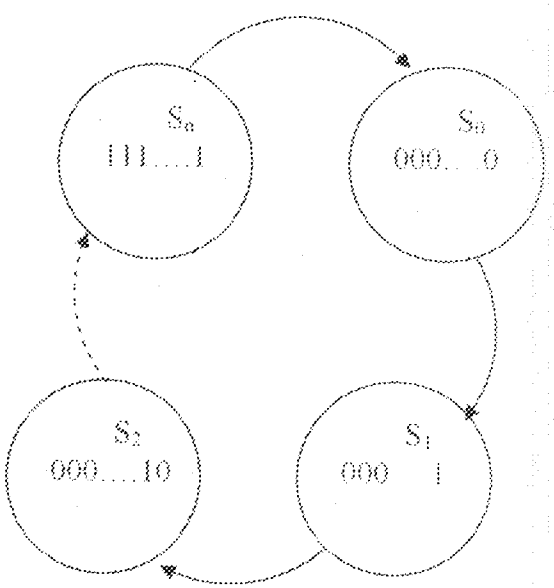



Fig 2.2: The State diagram of an n – bit counter

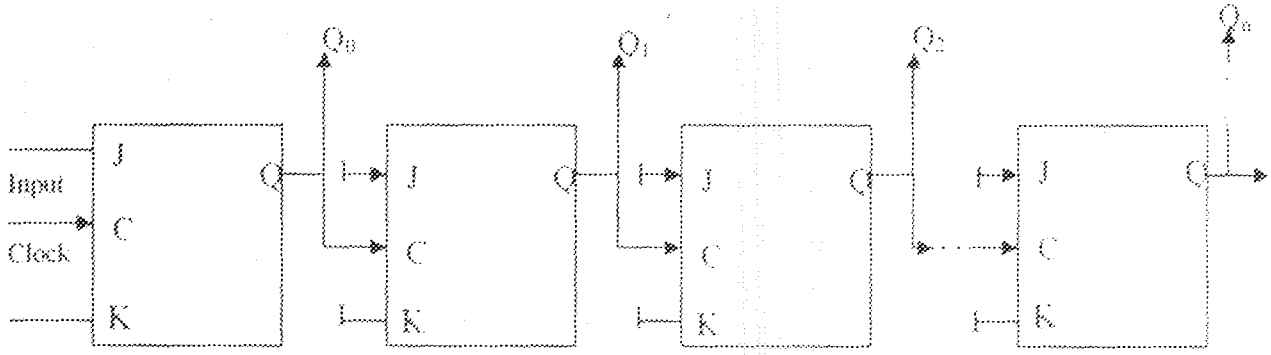



Fig 2.3: An n – bit asynchronous binary counter

### 2.2.3 MODULUS 10 ASYNCHRONOUS COUNTER

It is also called a BCD counter. It is a sequential counter that counts through a series of 10 distinct states before recycling. The figure 2.4 shows the design for a BCD counter.

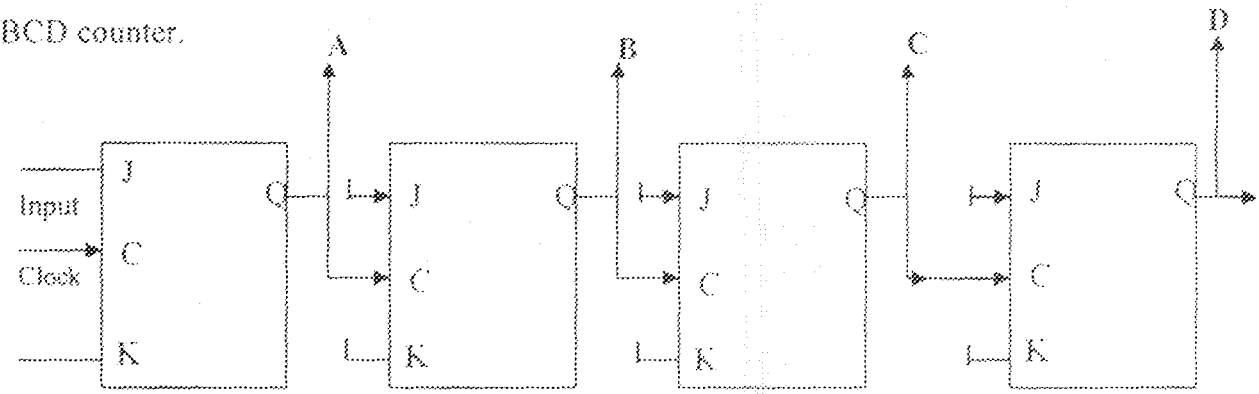



Fig 2.4: BCD asynchronous binary counter

Figure 2.4 is an asynchronous counter since the count input is not connected to the clock input of all the J – K flip-flops in the circuit. The first flip-flop has both J and K input tied high. So this flip-flop toggles with every input pulse to its clock input. The second flip-flop is more complicated. Its K input is tied high, but its J input comes from the reset output of flip-flop D. This means that, as long as the count is 0111 or less, the J input of flip-flop B will be high. Since the clock input of flip-flop B comes

from the set output of flip-flop A. Flip-flop B will toggle every time flip-flop A resets until the count gets to 1000. Flip-flop C ha both its J and K input tied high, and its clock input comes from the set output of flip-flop B. Thus flip-flop C will toggle every time flip-flop B resets. Finally, we come to flip-flop D. Its clock input comes from the set output of flip-flop. The K input of flip-flop D is tied high, but the J input comes from the AND gate of the set outputs of flip-flops B and C. Thus flip-flop D can only be set when both flip-flop B and C are also set.

It is common to gang several modulus 10 asynchronous counter together to form many digit decimal counter. The output from flip-flop D of one counter is tied to the count input of the next higher counter, hence giving the required member of modulus counter. [1, 2].

### 2.2.4 MODULUS - 1000 ASYNCHRONOUS COUNTER

A modulus 1000 asynchronous counter counts from decimal number 0 through 999. This actually required ten (10) JK flip-flops for the operation. In the absence of a single chip involving 10 JK flip-flops, three modulus – ten (10) counter may be employed. In this case, the most significant bit of the east significant modulus – 10 counter is used to clock the next least significant modulus – 10 counter and the most significant bit of this is used to clock the next modulus 10 counter. This is shown in figure 2.5.

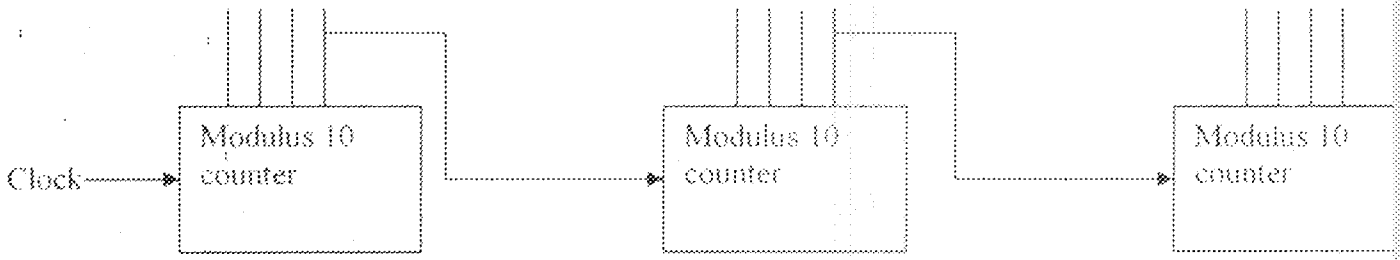



Figure 2.5: Using 3 modulus 10 asynchronous counter to realise a single modulus 1000 asynchronous counter

# CHAPTER THREE

# DESIGN AND IMPLEMENTATION

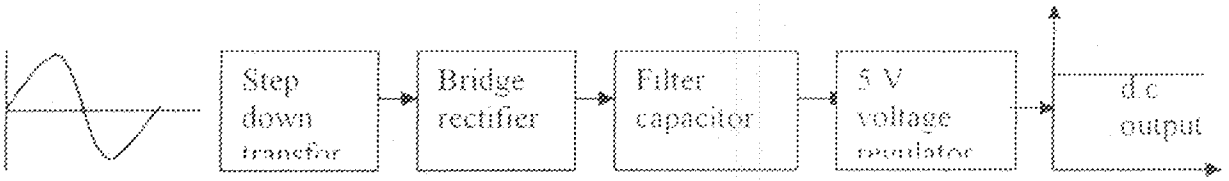
## INTRODUCTION

In order to design and analyse the entire circuitry properly, it was broken down into sub systems. Each of these sub systems is further sub-divided into parts to ease design and enhance explanations and understanding.

## 3.1 POWER SUPPLY UNIT

The purpose of regulated power supply is to provide constant 5V d.c. to power the system. No matter how much current is drawn by the load, the voltage is expected to be constant. Also variation in AC voltage, temperature and time passes should not affect the output voltage of the regulated power supply.

Figure 3.1 shows the block diagram and the circuit diagram of the regulated power supply.



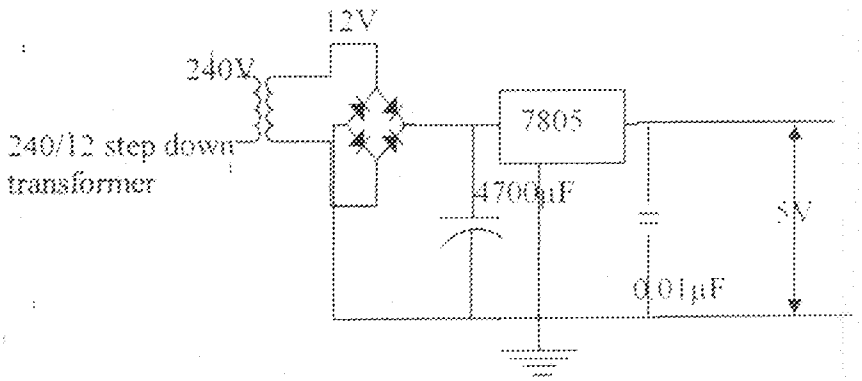




Fig 3.1: Regulated power supply circuit

### 3.1.1 TRANSFORMER

The transformer is a step-down type rated 240/12V, 300mA. This implies that whenever 240V a.c mains supply is applied to the primary of the transformer, a 12V a.c will be obtained at the secondary side of the transformer.

From the rating of the transformer, the voltage transformer turns ratio ($R_T$) can be calculated as:

$$R_T = \frac{\text{Secondary voltage}(V_s)}{\text{Primary voltage}\,(V_p)}$$

where $V_s = 12V$ and $V_p = 240V$

Therefore, $R_T = \frac{12}{240} = \frac{1}{20}$

∴ Transformer ratio $R_T = 20:1$

The transformer form factor $F = \frac{V_{rms}}{V_{dc}}$ [8]

But $V_{rms} = \frac{V_{max}}{\sqrt{2}}$

$V_{max} = V_{rms} \times \sqrt{2} = 12 \times \sqrt{2} = 16.97V$

Therefore $F = \frac{V_{max}/\sqrt{2}}{2V_{max}/\pi} = \frac{\pi}{2\sqrt{2}}$

### 3.1.2 BRIDGE RECTIFIER [8]

This employs four diodes to convert a.c voltage into pulsating d.c voltage. The following advantages are considered in selecting this design.

1. Much smaller transformers are required
2. It has less peak inverse voltage (PIV) rating per diode.
3. It is suitable for high – voltage application
4. No centre – tap is required on the transformer

The circuit diagram for a bridge rectifier is shown in figure 3.2

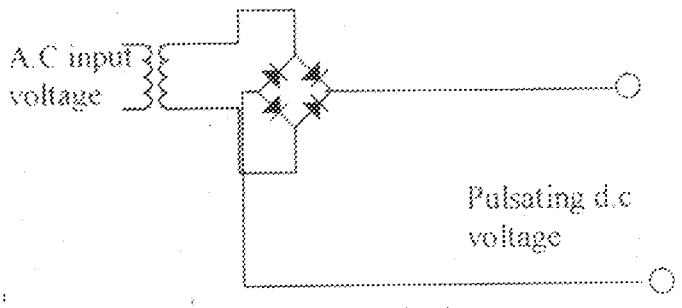



Fig 3.2: Bridge rectifier circuit

Rectifier efficiency,

$$\eta = \frac{\text{d.c power}}{\text{r.m.s power}} \times 100\% \quad [8]$$

$$\Rightarrow \eta = \frac{\text{d.c voltage, } V_{dc}}{\text{r.m.s power}} \times 100\%$$

using the rating of the transformer

$V_{rms} = 12V$

$V_{dc} = V_{rms}$ / form factor (F)

$$= \frac{V_{rms}}{\pi/2\sqrt{2}} \Rightarrow V_{rms} \times \frac{2\sqrt{2}}{\pi}$$

$$= 12 \times \frac{2\sqrt{2}}{\pi}$$

$V_{dc} = 10.8V \cong 11V$

$$\text{Therefore } \eta = \frac{10.8}{12} \times 100\%$$

$$= 90\%$$

Ripple content of the pulsating d.c output, $V_L$ (a.c)

$$V_{L(a.c)} = \sqrt{V_L^2 - V_K^2(d.c)} \qquad [8]$$

where $V_L = V_{rms} = 12V$

$V_{L(d.c)} = 10.8V$

Now $V_{L(a.c)} = \sqrt{12^2 - 10.8^2}$

$V_{L(a.c)} = \sqrt{27.36} = 5.23V$

Therefore, Ripple factor $\gamma$

$$\gamma = \frac{V_{L(a.c)}}{V_{L(d.c)}} \qquad [8]$$

$$= \frac{5.23}{10.8} = 0.484$$

= 48.7%

### 3.1.3 FILTER CAPACITOR

The main function of the filter capacitor is to minimise the ripple content in the rectified output voltage. This capacitor is connected across the rectifier output and in parallel with the voltage regulator as shown in figure 3.1.

The filter circuit depends for its operation on the property of a capacitor to charge up during conducting half cycle and discharge during the non – conducting half cycle. A capacitor opposes any change in voltage. When connected across a pulsating d.c voltage, it tends to smoothen action of the simple capacitor filter in a full wave rectifier.

**Effect of increasing filter capacitor**

Increase in the capacitor size

(1) increases $V_{dc}$ toward the peak rectified output voltage.

(2) reduce the magnitude of ripple voltage,

(3) increase the peak current in the diode

(4) reduces the time of flow of current pulse through the diode.

**Filter design calculation**

Minimized pulsating d.c output of the capacitor $V_{dc}$

$$V_{dc} = \frac{V_p}{1 + I_{dc} / 4F_c V_p} \qquad [8]$$

$$I_{dc} = \frac{V_{dc}}{R_l}$$

$$\Rightarrow V_{dc} = \frac{V_{ip}}{\left[1 + \frac{V_{dc}}{4F_c R_L V_{ip}}\right]}$$

where f = line frequency = 50 Hz

C = capacitance of the capacitor = 4700μF

$R_L$ = Resistive load connected in series to the seven segment display = 330 x 21 = 6930Ω

$\Rightarrow R_L = 6930\Omega$

$V_{ip}$ = peak rectified output voltage

$\Rightarrow V_{ip} = \sqrt{2} \times V_{(a.c)}$

$= \sqrt{2} x 12$

$= 16.970V$

Now $V_{dc} = \frac{16.970V}{\left[1 + \frac{V_{dc}}{4 \times 50 \times 4700 \times 10^{-6} \times 6930 \times 16.97}\right]}$

$$V_{dc} = \frac{16.97}{1 + 9.0 \times 10^{-6} V_{dc}}$$

$\Rightarrow V_{dc} + 9.0 \times 10^{-6} V_{dc} = 16.97$

$\cong 9 \times 10^{-6} V_{dc} + V_{dc} - 16.97 = 0$

Therefore

$$V_{dc} = \frac{1 \pm \sqrt{1 + 0.000009 \times 4 \times 16.97}}{0.000009 \times 2}$$

$$V_{dc} = \frac{3.05 \times 10^{-4}}{1.8 \times 10^{-5}}$$

$V_{dc} = 16.94$

Ripple factor of the pulsating filtered d.c output γ

$$\gamma = \frac{1}{4\sqrt{3} F_c R_L} \qquad [8]$$

$$\gamma = \frac{1}{4\sqrt{3} \times 4700 \times 10^{-6} \times 6930}$$

$$\gamma = \frac{1}{225.658}$$

$$\gamma = 4.431 \times 10^{-3}$$

$$\equiv 0.443\%$$

Ripple content of the output filtered $V_{r\,(rms)}$?

$V_{r\,(rms)} = \gamma V'$ dc [8]

$V_{r\,(rms)} = 4.431 \times 10^{-3} \times 16.94$

$= 0.075$Volt

### 3.1.4 VOLTAGE REGULATOR

A 7805 voltage regulator integrated circuit was used to reduce variation between no load and full bad condition to zero or at least minimum possible value. The voltage regulator circuit is shown in figure 3.3.

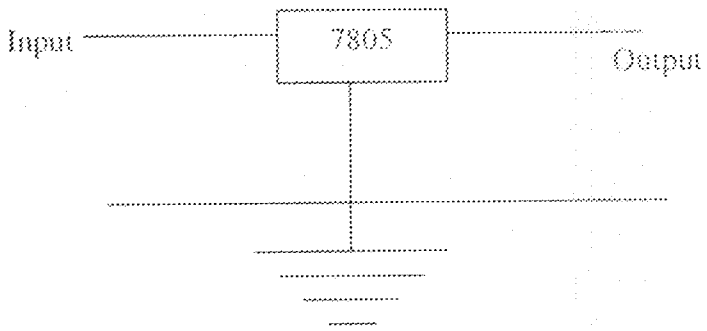



Fig 3.3: A 7805 voltage regulator

To ensure constant 5V output, the input voltage ranges from the minimum value of +7V to 35V.

### 3.2 MANUAL PULSE GENERATOR UNIT

The square wave pulse is generated with the use of a stable circuit. The 8 – pin 555 timer is used in this project. The astable circuit uses a regulated 5V supply. The figure 3.4 shows the actual arrangement of 555 timer.

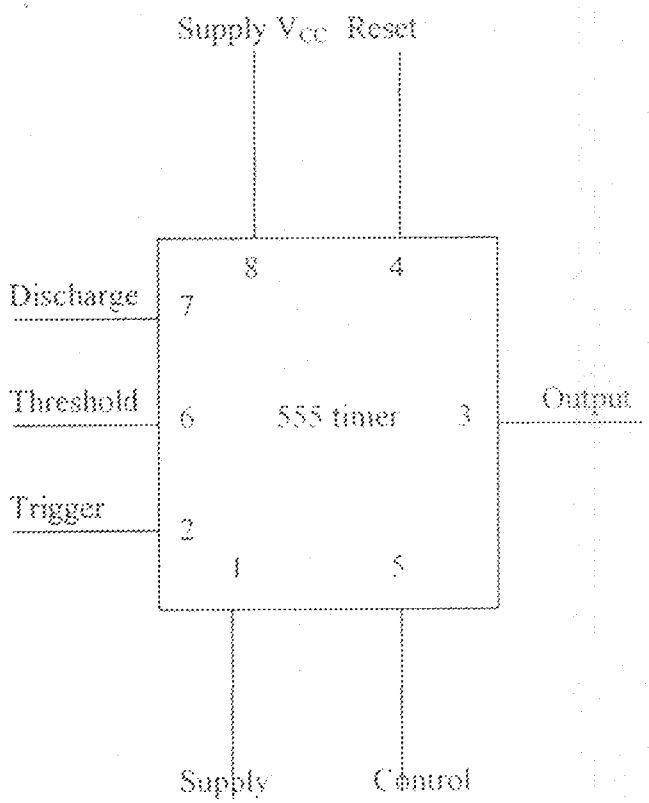


Fig 3.4: Actual pins arrangement of 555 timer

### 3.2.1 555 ASTABLE CIRCUIT

An astable circuit produces a square wave, which is a digital waveform with sharp transition between low (OV) and $+V_{CC}$. The duration of the high and low state may be different.

The time period (T) of the square wave is the time for one complete cycle. It is usually better to consider the frequency (f) which is the number of cycles per second.

The figure 3.5 shows how the 555 timer is connected to generate pulses for the three digit counter.

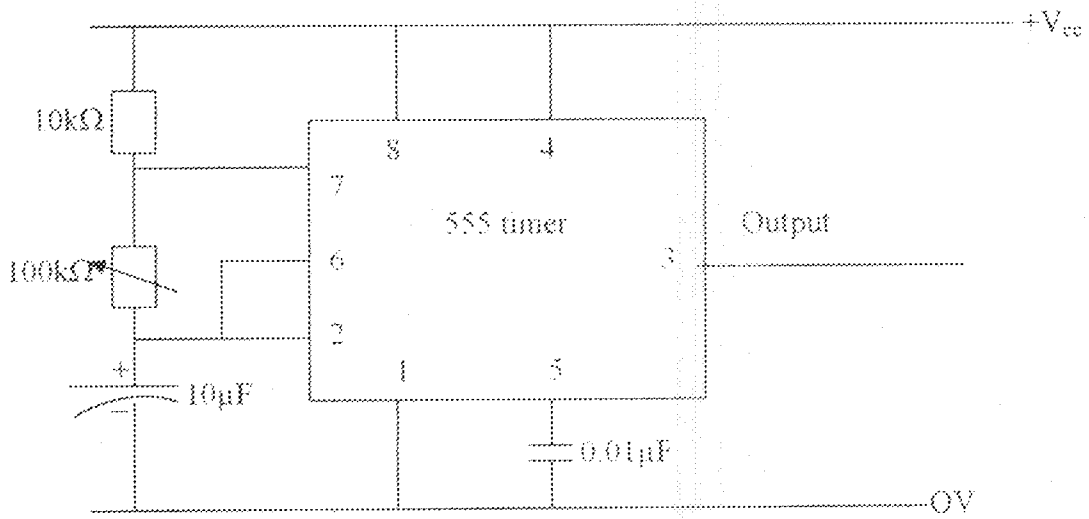



Fig 3.5 pulse generator circuit

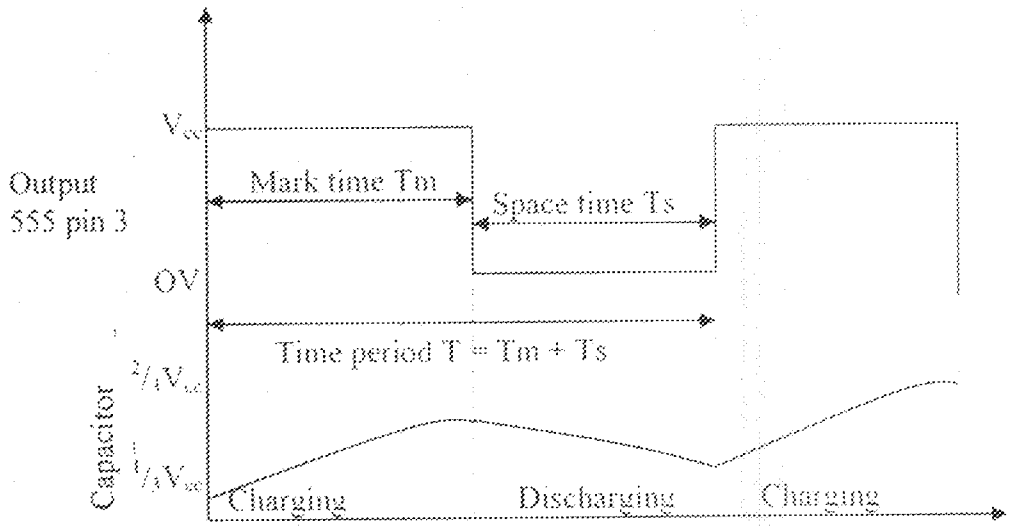



Fig 3.6 Output Wave form

With the output high ($+V_{cc}$) the capacitor $C_1$ is charged by the current flowing through $R_1$ and $R_2$. The threshold and trigger input monitor the capacitor voltage and when it reaches $^2/_3$ $V_{cc}$ (supply voltage), the output becomes low and the discharge pin is connected to the OV (ground).

The capacitor now discharges with current flowing through $R_2$ into the discharge with current flowing through $R_2$ into the discharge pin. When the voltage falls to $^1/_3$ $V_{cc}$ (trigger voltage), the output becomes high again and the discharge pin is disconnected allowing the capacitor to start changing again. the cycle repeats continuously unless the

$= 1.076\text{Hz}$

$f \cong 1.08\text{Hz}$

Since the variable resistor is used in the project design, we can vary the value of resistor, ranges from $1.00 \leq R_2 \leq 100\text{k}\Omega$

The table 3.1 shows the different frequencies by varying the value of $R_2$ using the constant value of $R_1 = 10\text{k}\Omega$ and value of capacitor $C_1 = 10\mu\text{F}$

Table 3.1 Different frequency by varying the $R_2$

| $R_2$ (k$\Omega$) | Frequencies (Hz) |
|---|---|
| 20 | 2.8 |
| 40 | 1.55 |
| 60 | 1.08 |
| 80 | 0.82 |
| 100 | 0.68 |

Since the frequency (f) which is 1.08Hz is the number of circle per second, therefore, the number of cycles per minute is $1.08 \times 60 = 64.6$ per min $\cong 65$ per min.

## 3.3 DECADE COUNTER

The counting function is a very important one in digital system. This converts events or pulses generated from the generator circuit to a particular code sequence. In order for a counter to perform its function properly, it must have the ability to remember the present number, so that is can move on to the next proper number in sequence. Therefore storage capacity is an important characteristic of all counters; and, flip-flop are

normally used to implement them. A counter is a special type of sequential circuit with a single clock input and number of outputs. Each time the counter is clocked, one or more of the output change state The counter used for this design is referred to as a decade counter, which can be constructed from four flip-flops and a gate.

Counter can be divided into two categories namely: synchronous and asynchronous (ripple) counter. The synchronous counter clocks all the flip-flop simultaneously, whereas in ripple counter each stage is clocked by the output of the previous stage [5].

### 3.3.1 ASYNCHRONOUS (RIPPLE) COUNTER

For a four state BCD counter consisting of four flip-flops, the output of the last propagation delays a negative edge of the input clock.

The ratio of the input frequency to the output frequency of a counter is called the modulus. The counter required for this project is mod – 10 counter and as such counts in sequence from 0000 to 1001 that is 0 to 9. Asynchronous decade counter flip-flop cascade is shown in figure 3.7.

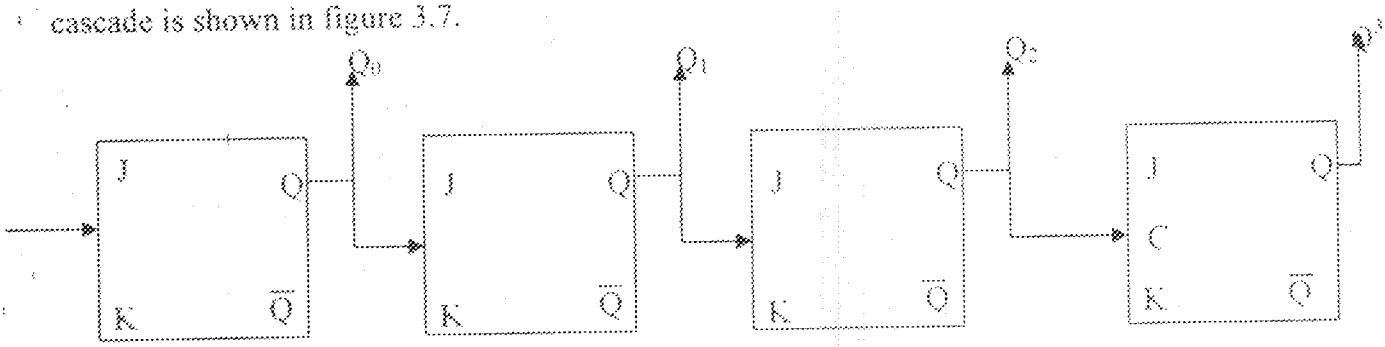



Fig 3.7 An asynchronous decade counter

The truth table for the counter above is shown in the table 3.2. Below the weighted

binary value of the outputs $Q_0$, $Q_1$, $Q_2$ and $Q_3$ gives a value equivalent to the decimal. Since the count is from 0 to 9 inclusive in this case, then the unique representation of the four bits to an equivalent decimal number can be utilized to give a visual indication of the decimal count. The use of the four bits in this way gives a binary coded decimal count (BCD) [1].

Table 3.2: The truth table of asynchronous decimal counter

| CLK | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |

The 7490 is a 4 – bit ripple counter. However, its flip-flops are internally connected to provide MOD 2 (count to 2) and MOD – 5(count 5) sections. Again each section uses a separator clock pin 14, CPO for MOD – 2 and pin 1, OPI for MOD – 5. By connecting $Q_0$ (pin12) to CPI (pin 1) and using CPO (pin4) as the single clock input, a MOD 10 counter (decade or BCD counter) can be created. The 7490 IC is a 14 pin DIP type having input voltage of +5V is shown in figures 3.8.

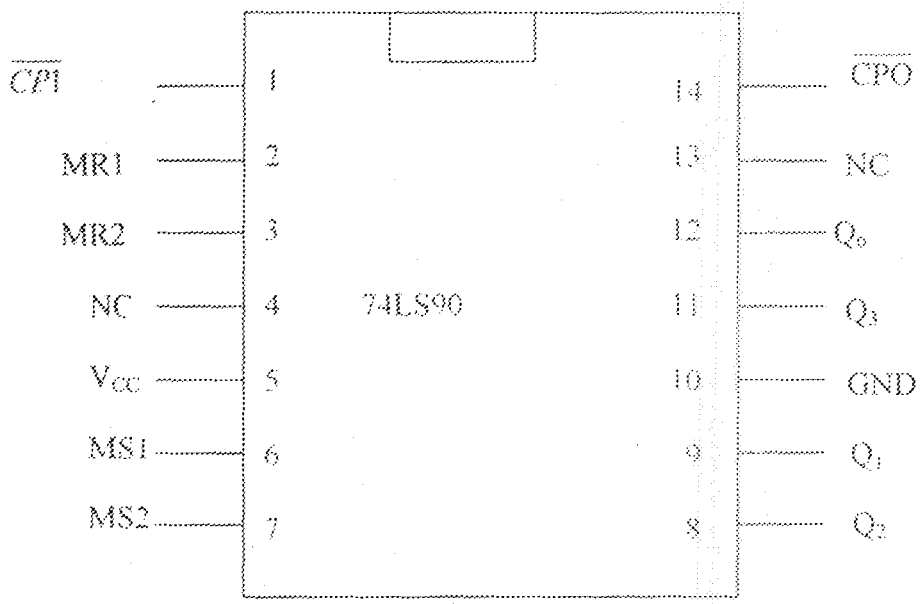



Fig 3.8 Schematic diagram of 74LS90

The figure 3.9 shows the way of connection or combining counters. This project used three 7490 MOD 10 counters IC which are cascaded together to create a three digit (decimal) counter as shown in fig 3.9.

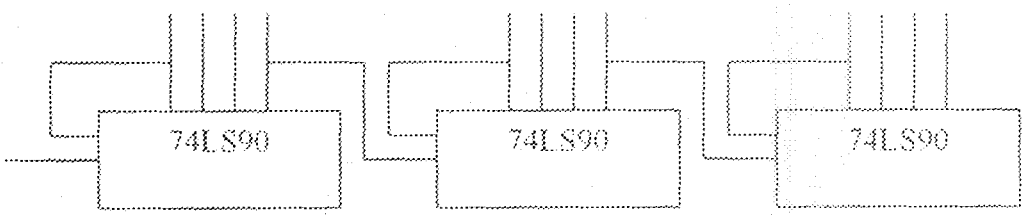



Fig 3.9: Three decade counter cascaded to form three counter

## 3.4 BCD DECODER/DRIVER

This converts coded information such as binary number into a number coded form such as decimal form. For example, a particular type of decoder/driver accepts BCD code applied to its inputs and provides output to energise the 7 – segment display device to produce digital read out. The BCD-to-7-segment decoder/driver used in this project is the 7448 IC. The IC is a 16 pin DIP type having input voltage of 5V. The 7448 is a device that more than one output can be driven low at a time. This is important because it allows the 7448 to drive a 7 segment LED display, to create different numbers, it is necessary that it drive more than one LED segment at a time. For example, in figure 3.4a, when the BCD number 5 (0101) is applied to the 7448's inputs, all the output b and e go low. This causes LED segment a, c, d, f, g to light up. The 7448 sinks current through their LED segment as indicated by the internal wiring of the display and the truth table. The BCD decoder/driver converts BCD data into the format suitable for producing decimal digits on common cathode LED 7 – segment display.

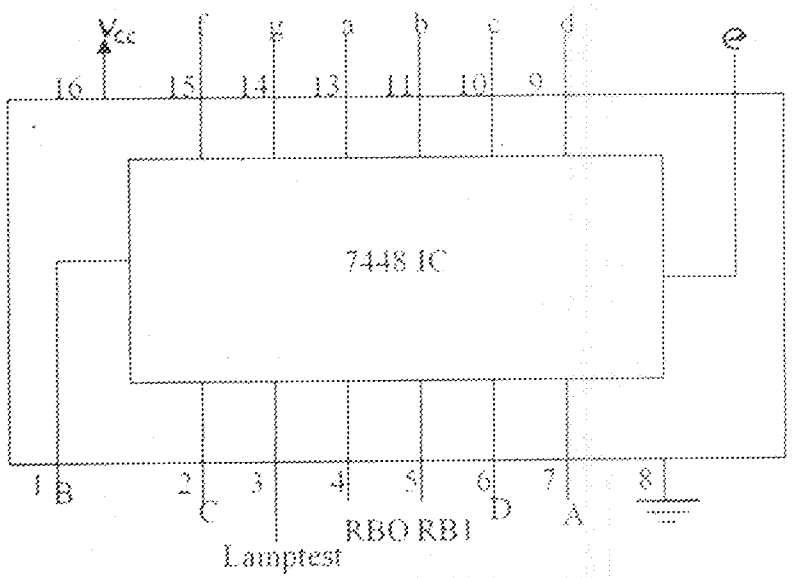



Fig 3.10: Schematic of the 7448 decoder

Table 3.3: Truth table for the 7448 integral circuit

| A | B | C | D | Decimal digits | g | f | e | d | c | b | a |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 2 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 3 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 4 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 5 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 6 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 7 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 9 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

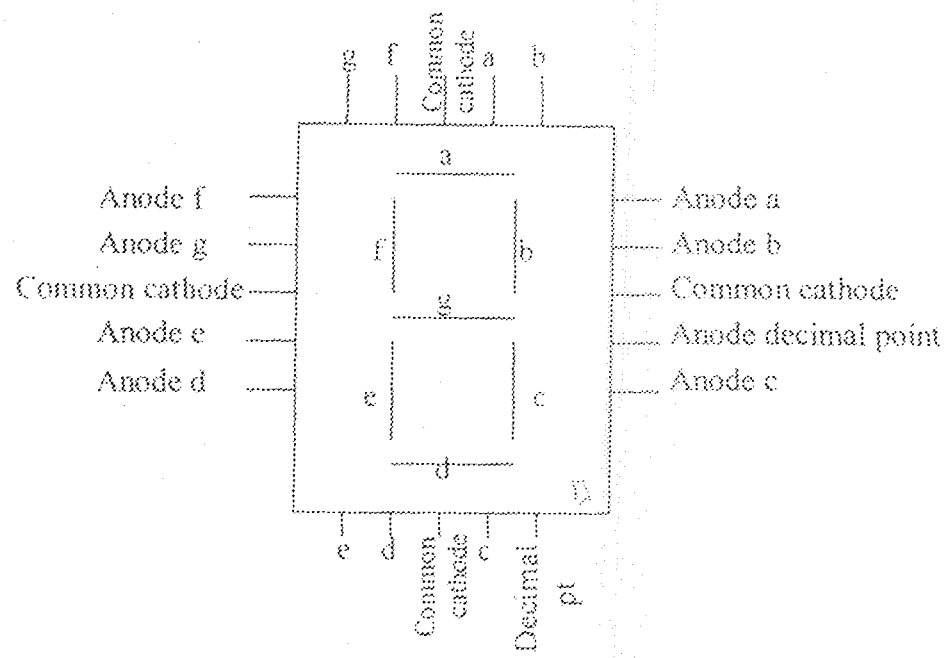
The 7448 also comes with a lamp test active low input (LT) that can be used to drive all LED segment at once to see if any of the segments is faulty. The ripple blanking input (RB1) and ripple blanking out (RBO) can be used to multistage display application to suppress a leading edge and or trailing edge zero in a multi digit decimal.

## 3.5 SEVEN SEGMENT DISPLAY

Seven segment displays are used to convert 4-bit BCD number into a visible readout LED. It is commonly used, because of its brightness, low cost, reliability and

compatibility with low voltage integrated circuit. In a typical seven-segment displays, each segment may be connected as a common anode display in which the positive side of the power supply is connected to the anode of each segment and a low voltage (OV) at the segment cathode lights the segment or they may be connected as a common cathode display in which the negative side of the power supply is connected to the cathode of each segment and a high voltage (1) on the ground anode lights the segment. To control the display, we must generate a 7 bit code to indicate which segment showed be on or off. If we let 0 correspond to OFF and 1 to ON that is common cathode as used in this project work, the seven-segment code for the decimal digits is shown in the table 3.2 [10].

Most digital equipment have some means for displaying information in a form that can be understood readily by the users or operator. Seven segment displays are used in almost every electronic digital system from electronic digital clocks the electronic scoreboaeds. A seven-segment display can be used to produce any digit 0 – 9, along with a very limited number of letters by energizing certain combination of the segment certain combination of the segment. One common arrangement uses light – emitting diodes (LEDs) for each segment. By controlling the current through each LED, some segments will be dark so that the desired character pattern will be generated. Figure 3.11 shows the common cathode seven segment display used for this project work.




[1, 9]

Fig 3.11: Typical pin connection of common cathode 7- segment LED

The figure 3.12 shows the pin output from the 7448 IC to seven-segment decoder/driver, (the arrangement used in the project) being used to drive a seven-segment LED readout. Each segment consists of one or two LEDs, the cathodes of the LEDs are tied to Vcc (+5V)(common cathode). The anode of the LEDs are connected through current limiting resistor to the appropriate output of the decoder/driver.

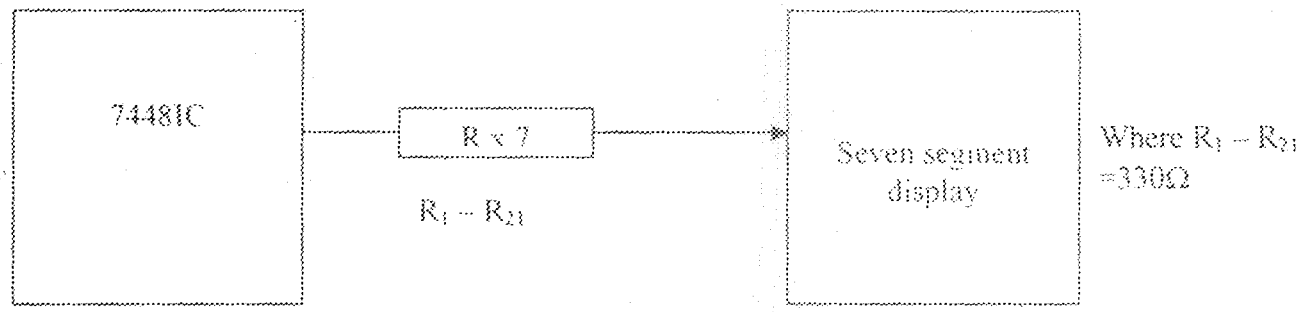



Fig 3.12 BCD decoder/driver connected to seven segment display

The active segment for each decimal digit are shown in the table 3.4.

Table 3.4: Active segment for each decimal digit

| Digits | Segment selected |
|---|---|
| 0 | a, b, c, d, e, f |
| 1 | b, c |
| 2 | a, b , d, e, g |
| 3 | a, b, c, d, g |
| 4 | b, c, f, g |

| Digits | Segment selected |
|---|---|
| 5 | a, c, d, f, g |
| 6 | a, c, d, e, f, g |
| 7 | a, b, c |
| 8 | a,b, c, d, e, f, g |
| 9 | a, b, c, d , f, g |

The limiting resistors are connected in series with the seven segment display as shown in figure 3.13.

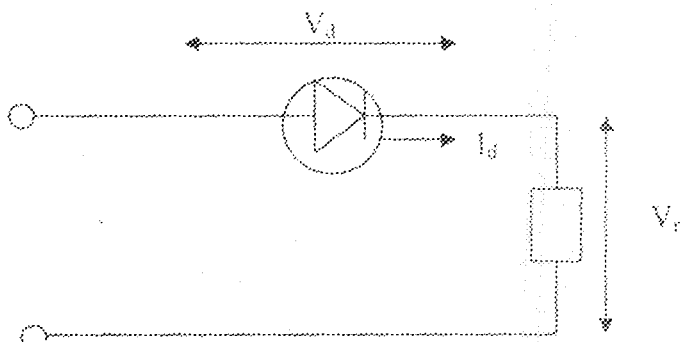



Fig 3.13: Series connection of resistor with seven segment display

The range of voltage drop in the diode is $1.0 \leq V_d \leq 3.0$ when the supply voltage is 5V, limiting resistors is:

$$\text{Limiting resistor} = \frac{V_r}{I_d} = \frac{V_s - V_d}{I_d} \qquad [11]$$

Assume the $V_d = 1.7V$, the current flowing through the diode $I_d$ is 10mA.

Therefore, limiting

$$\text{Resistor} = \frac{V_s - V_d}{I_d} = \frac{5 - 1.7}{10 \times 10^{-3}}$$

$$\text{Limiting resistor} = \frac{3.3\times10^{3}}{10} = 330\Omega$$

Therefore $R_1$ to $R_{21}$ = 330Ω each

## 3.6 CONSTRUCTION

The design specification of each component was followed strictly except in case of non – availability of components. In such cases, changes in design specification were done. To ease construction procedure, the project circuitry was segmented and divided to ease the construction problem. The construction includes a prototype on the temporary location of breadboard and then proper construction of the completed design on the vero board.

### 3.6.1 COMPONENT LAYOUT

A layout plan for the component location on vero board was drawn on paper. The plain paper component layout helped to ensure proper location for the ICs, the number of ICs the board can accommodate, the proper and the best route for connection between each IC and the components and the position of the switches and push buttons.

The segments (Modules) in which the circuitry was reduced to ease up construction includes: power supply unit, pulse generator, decade counter, BCD decoder/driver and seven segment display.

### 3.6.2 HARDWARE CONSTRUCTION

Preliminary construction and connection of the different components was carried out according to design on the breadboard. Each module was tested and result obtained before transferring unto the vero board for permanently and firm soldering. After every connection had been done and cross checked for any open or short circuit, the circuit was tested again.

### 3.6.3 SOLDERING

Soldering was achieved with the use of soldering iron, soldering lead and a plastic solution tube. Some extra care taken during soldering are given below:

1. Care was taken to ensure proper contact while using little but enough soldering lead for the joints.
2. Easier and faster soldering was ensured by thinning the terminals of the components with melted soldering lead.
3. To protect active components such as IC, IC sockets were used.
4. Care was taken to ensure soldering iron temperature was not too high so as to protect the component from damage by overheating.

### 3.6.4 TOOLS USED IN DESIGN AND CONSTRUCTION

1. Computer software (multisim) was used to model the circuit, it was simulated and tested to ensure proper logic connection.
2. Initial construction was carried out on the breadboard. On transferring to the vero board, care was taken to ensure proper soldering between junctions.

3. Soldering iron and soldering lead was used in soldering the component on the vero board.
4. Digital multimeter were used to carry out the test including continuity, voltage measurement, resistance, capacitance and current at various point on the circuit.
5. Suction tube was used to suck soldering misplaced lead from the board to avoid short circuit and ensure clean construction.

# CHAPTER FOUR

# TEST, RESULT AND ANALYSIS

## 4.1 TEST ANALYSIS

Proper care was taken to ensure neat and firm connection. Having completed the construction, a careful test and assessment of all the components connection was carried out as follows:

1. The continuity and connectivity of the connecting wires and links were taken while not powered, using the multimeter.
2. Testing different section of the construction, from one stage to another.
4. Polarities of polarized components were tested.
5. Making sure that all appropriate components were properly powered, taking into account positive and negative leads of supply.

## 4.2 RESULT

From the design, analysis construction and testing, it can be concluded that the project circuiting design performed very well according to design. The manual mode three digit counter constructed from the principle of digital timing and use of counter can be used to count and display them numerically.

## 4.3 DISCUSSION

After the construction and testing, the device was powered and tested in full operation. The transformer provides the AC voltage of 12V input; this is reduced to a regulated 5Vdc for powering of digital component. At initial power up, the reset button is

pressed and the count read 000. The counter does not start to count until the push button is pressed manually. The counter is observed to stop the count of the clock pulse whenever the push button is released.

# CHAPTER FIVE

# CONCLUSION AND RECOMMENDATION

## 5.1 CONCLUSION

The aim and objective of this project work has largely been achieved, that is to design construct a low cost, simple, successfully as described in the preceding chapters.

This adventure into the field of digital counting, number system can also serve as stimulant for others who will consider undertaking project topic related to it. The objectives and its focus over to meaningfully contribute to the economy of the country and provide convenience and accuracy of counting people in a given gathering by manually pressing the push button and release it. The following integrated circuits: 7805IC, 555 timer, 74LS 90, 74LS 48 and common cathode seven – segment display.

## 5.2 PRECAUTION

- It was ensured that all components were tested on the breadboard.
- It was ensured that the tested results were corresponded to the design specification with measurements by multimeter before transferring to final circuit board (vero board).
- It was ensured that the pins of the ICs were properly connected in the appropriate way to the already soldered IC sockets.

## 5.3 RECOMMENDATION

The design can be used to count manually by the press of a push button.

In view of the strategic importance of digital electronics in our lives today, the electrical control and comfort is of equal importance. Based on this are success and limitations recorded by the project work. The following recommendations are given:

1. Students should be encouraged to undertake research in digital electronics system in order to give them broad view into the possibilities of thing that can be achieved.

2. To ensure corrections and accuracy of count of people manually.

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Circuit Diagram of 4 BCD Clock Display