DESIGN AND CONSTRUCTION OF DIMMER SWITCH USING REMOTE SYSTEM WITH DIGITAL DISPLAY UNIT.

BY

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97/5937

A PROJECT SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENT OF THE AWARD OF BACHELOR OF ENGINEERING (B.ENG) DEGREE IN THE DAPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING SCHOOL OF ENGINEERING AND ENGINEERING TECHNOLOGY, FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA, NIGERIA.

AUGUST 2003.

DECLARATION

I hereby declare that this project is the result of my hand work and research which has never been presented anywhere by anybody. I was under the supervision of my H. O. D. Dr. Y. A. Adediran in the department of Electrical and Computer Engineering of Federal University of Technology, Minna, Niger State.

.... 16/10/03. ....

Student — Date

Aliyu Solomon Yisah

CERTIFICATION.

This is to certify that this project titled Design and Construction of Dimmer Switch using Remote System with Digital Display Unit was carried out by Aliyu Solomon Yisah (975937) under the supervision of my H. O. D Dr. Y. A. Adediran and submitted to electrical and computer engineering department, Federal University of Technology, Minna in partial fulfillment of the requirements for the award of Bachelor of Engineering (B. Eng) degree in Electrical and Computer Engineering.

....

Dr. .Y. A Adediran Date

(Project supervisor)

.... 7/4/04

ENGR. M. N. NWOHU.

(Head of Department) Date

....

External Examiner Date

DEDICATION

This project work is dedicated to the Almighty God for His mercy, guidance and blessing over me.

ACKNOWLEDGEMENT

I am grateful to the almighty God who has given me the strength and courage in all my endeavours. I will like to express my profound gratitude to my Late father Barr. S. G. Aliyu for his love and financial support. Since the beginning of my academic pursuit.

I also appreciate the untiring support of my mother, Mrs. Martha Aliyu, my brother Friday Aliyu and my sisters, Mrs. Rachael Allasan, Cecillia Aliyu, Millicent Aliyu and Eunice Aliyu.

My thanks goes to my supervisor, Dr. Y. A. Adediran for sacrificing most of his time in advising and assisting me whenever I have problem on this project. I am also indebted to my friends on the campus and outside the campus, friends like Timuola Olorunishola, Mr. Abaka Musa, Engr. Joshua, Engr. Don, Engr. Segun, Mr. Voke and Engr. Ayo just to mention but few.

I will like to seize this opportunity to pray for those who have assisted me in one way or the other for successful completion of my programme at F.U.T Mina. May God Almighty be with everybody in all their endeavours, amen.

ABSTRACT.

The dimmer switch using infrared remote control with displace unit is a power control device, comprising a triac circuit used to give a sample on/off type of power control, in which either full or zero power is applied to a load.

There are three basic stages in this project. They are the dimmer switch, displace unit and the infrared remote control unit. The infrared system modulate the infrared light at around 36 – 40KHz (this is the frequency of infrared carrier and should no be confused with the actual frequency of the infrared light itself.)

The infrared remote control is 32 – 40KHz modulated square wave for communication. This square wave is then send to the infrared – amplitude modulated by the data, usually fully on/off type modulation, usually the transmitter part is constructed so that the transmitter oscillator which is driving the infrared – transmitter LED can be turned on/off by applying a TTL voltage on the modulation control input.

On the receiver side a photodiode take up the signal. The integrated circuit inside a receiving chip is sensitive only around a specific frequency in the 32 – 40KHz range. The output is the demodulated digital input, just what was used to drive the transmitter. The receiver works when infrared the carrier is present, this output is high. When no carrier is detected the output is low. And the output voltage is read-out with the help of the $3^1/_2$ digit 7 – segment displace.

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CHAPTER ONE

General Introduction

1.1 Introduction

Light is everything in your home. The light level in a room affects the way we do our work, and it has a huge effect on how we feel. It is difficult for us to read under a single candle, and a romantic dinner for two isn't so romantic under a 1, 500 watt halogen lamp.

The issue here is that we need to use some rooms for many different purpose, and different functions calls for varying amount of light. This is when the light dimmer switch comes into place; a handy electrical component that lets you adjust light levels from nearly dark to fully lit by simply turning a knob or sliding a lever.

An effective way to quickly change the mood of a room is by dimming or brightening the lights with a dimmer switch. A softer light results in a more comforting, relaxing atmosphere. Brighter lighting is more suitable for normal room use and reading. Any easy way to control your lighting is to install a dimmer switch.

1.2 Aims and Objectives.

The aim of this project is to design and construct a dimmer switch with digital display using remote control. It works as a high speed power switch which operates at a potential up to several hundred volts and can handle current up to tens or hundreds of amps.

It is intended that this project will be able to regulate the light intensity of a lamp or the speed of an electric motor by regulating the voltage.

Some current application of Dimmer switch systems are:-

Household application: Dimmer switches are used in our homes to dim electric lamp intensity and they are also used in electric cooker, electric fan.

Industrial application: Used in regulating the speed of an electric motors.

METHODOLOGY

This project contains three major building blocks each of which was designed separately using discrete components as well as IC's. These blocks are, light dimmer, remote control and display circuit.

The dimmer circuit is built around a unijunction transistor which forms a basic oscillator and generates pulses, which are generated by a capacitor placed at its gate in a voltage – divider connection with a resistor. The capacitor's charging and discharging are controlled by two transistor switches. The pulses generated by the unijuction transistor are applied to the gates of a triac which, in turn, is used to switch on the main load which is the bulb. A 250kΩ variable resistor is used to vary the phase at which this pulses are applied from 30^0 to 120^0 hence the circuit dimmer action.

The remote control is made up of two blocks. The transmitter, an oscillator in the transmitter built around a 555 timer generates 37KHz with a duty cycle $\leq$ 1 which are buffered through and emitter base follower and used in driving an infrared diode. The infrared diode send pulses at same frequencies.

The receiver circuit senses the infrared signals from the transmitter circuit through its infrared sensor (diode). This is made in such away that it conducts when infrared pulses fall on it. It is connected across the base of a transistor switch which switches on and off at the same rate at which the pulses are applied. The signals are further amplified by a two-stage transistor amplifier and filtered by a stage-to-stage capacitive coupling. Finally the pulse are shaped by IN4148 signal diodes which are connected as diode clamps.

The output pulses are fed into a decode counter 74LS93 which is connected in mode 10. The counter output binary numbers range from 0000 – 1010, which are fed into 4028 binary-to-decimal decoder this decoder out-put binary number from one to ten different transistors contained in a CA3046 transistor array the transistors through their collectors are used to select different voltage levels this replaces the 250kΩ resistor in the dimmer circuit.

The third block is the display circuit connected in parallel with the load to sense the output. This is attenuated by a simple voltage divider method to give one volt at 300v the one volt is fed into a precision amplifier built around 741IC. The output which is half-wave is fed into an integrator within output as a full-wave rectified one volt and which can be adjusted to 2v the output is sensed and displayed by an analogue-to-digital counter, 7106IC. This is an IC having counters, seven segment decoders, latches and logic blocks. It directly drives a $3^1/_2$ digit display and needs no transistor drives. The load voltage at every level of attenuation is displayed on seven-segment display

1.4 Literature Review.

Light dimming is based on adjusting the voltage that gets to the lamp to emit only small amount of light. Light dimming has been possible for many decades by using adjustable power resistors and adjustable transformers. Electronics controlling also made possible to make them easily controllable from remote location.

Years ago, this was done using rheostat a large variable resistor. This method wasted electricity and generated a lot of heat. To control the amount of energy going to the light the rheostat had to throw a lot away, turning it into heat. For example, at half brightness a 100watt bulb would waste about 20 watts to heat in the rheostat.

Modern dimmers take a more efficient approach. Instead of diverting energy from the light bulb into a resistor, modern resistor rapidly shut the light circuit off and on to reduce the total amount of energy flowing through the circuit.

Modern light dimmer switches use a transistor – like device called a TRIAC to switch the electricity on and off very rapidly. Because the sort of 'chop up' the electrical power this way they are sometimes called 'chop switches.' The current doesn't change suddenly. It rises and fall or undulates.

1.5 Project Outlines

This project is divided into four chapters:

Chapter one discusses general introduction of the project, some of the current application of dimmer switch systems, the aims and objects of the project, the methodology employed in carrying out the project and literature review.

Chapter two is on system designs. Here calculations leading to the choice of component used are shown. Chapter three is assigned with construction, testing and results. The method of construction and the construction of the boxes containing the circuit are discussed here.

Chapter four is for conclusion and recommendations.

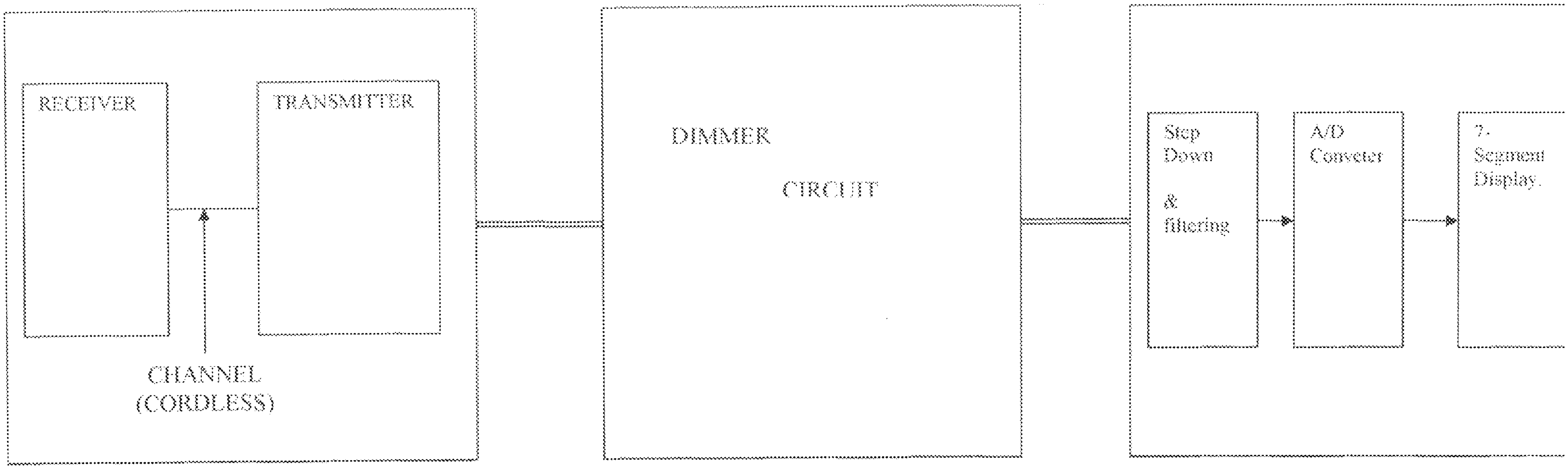


FIG 1 SYSTEM BLOCK DIAGRAM

CHAPTER TWO

System Design

2.1 The Power Supply Unit

The A/D converter used in this project design required a dual voltage supply of 15v. The connection of the power supply unit is shown in figure 2.1. The circuitry consists of 12v center tap transfer whose output are fed into the diode bridge rectifier to produce a dc voltage output some capacitors of specified capacitance values were used to remove ripples by way of filtering. The 7805 and 7905 IC voltage regulators were used to produce constant dc voltage supply of +5v and -5v respectively which is required to power the op-amp IC chips used in the project and to drive ICL 7107 A/D converter. The positive 5v and negative 5v supply from the supply unit are connected at pin 1 and pin 26 respectively of the ICL 7107 A/D converter, while pin 21 is grounded.

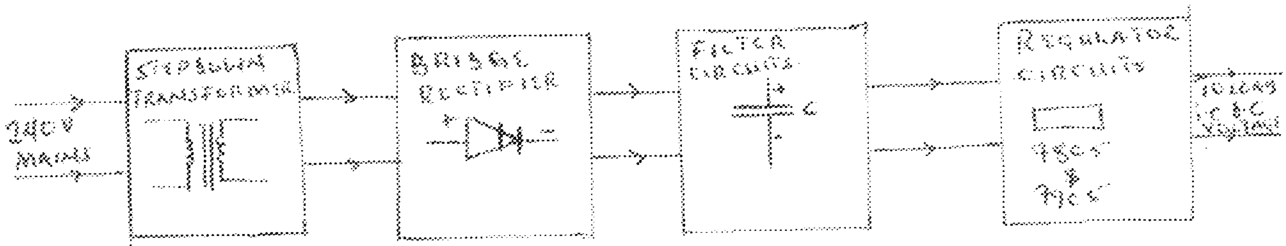


Fig 2.1

THE BLOCK DIAGRAM OF A POWER SUPPLY

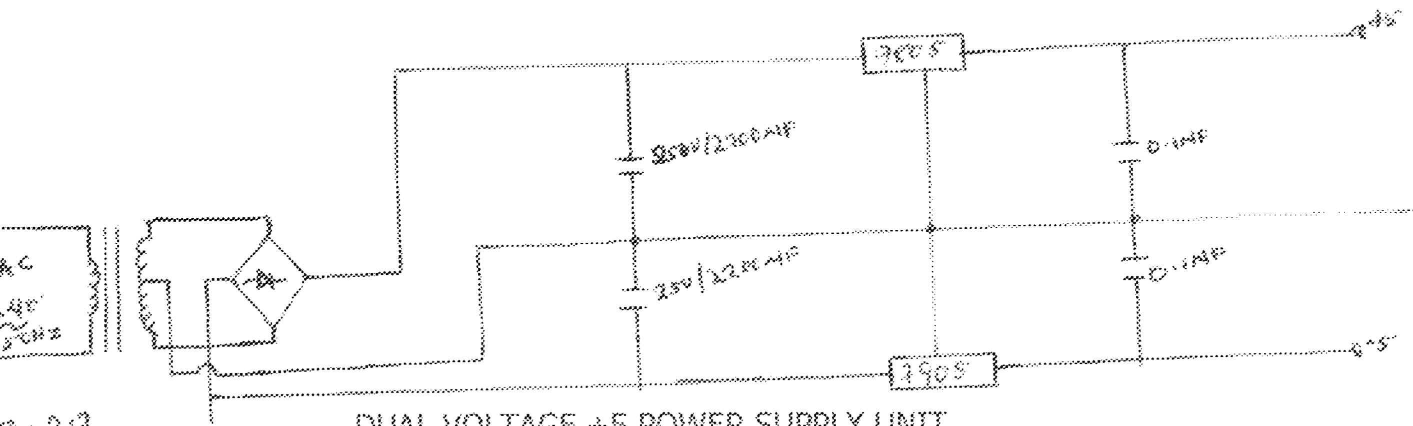


Fig 2.2

DUAL VOLTAGE ±5 POWER SUPPLY UNIT.

Transformer selection

$P_o = Vdc$ x Idc

$= 2V_m / \bar{A}$ x $2I_m / \bar{A}$

$= 2\sqrt{2}$ Vrms/$\bar{A}$ x $2\sqrt{2}$ Vrms/$\bar{A}$ x Vrms/R

$= 8Vrm^2s / \bar{A}^2 R$

Therefore Vrms $= \sqrt{P_o \bar{A}^2 R/8}$

for this project

P_o is 9W, $R_L = 9\Omega$

Vrms $= \sqrt{9 \times \bar{A}^2 \times 9/8}$

$= 9.9914V$

$\approx 9V$

ii. *Diodes rating*

Voltage rating: the maximum voltage, which occurs across the diode in the reverse direction, peak inverse (PIV) must be less than the break down voltage of the diode if it not conduct appreciably in the reverse direction.

For a full - wave,

PIV = $2V_M$

$V_M = \sqrt{2}$ Vrms

$\sqrt{2} \times 12$

$= 16.197V$

$V_M \approx 17V$

Therefore PIV = 2 x 17

= 34V

The breakdown voltage must be greater than PIV (Bdv > PIV)

iii. *Capacitor Selection*

Voltage rating

Capacitor voltage, V_c rating $\geq \sqrt{2}$ Vrms

$\sqrt{2} \times 12$ = 16.97V ($\sqrt{2}$ Vrms)

$V_C \geq \sqrt{2}$ Vrms

$V_C \geq 16.97V$

Therefore a capacitor of voltage rating of 25v was chosen.

Capacitance rating:

$\Delta V = V_M / 2FRC$

$\Delta V \alpha 1/C$

If a peak - to - peak ripple voltage of not more than 10v is to be tolerated.

$10 = 12\sqrt{2} / (50 \times 8 \times C)$

$C = 12\sqrt{2} / 8000$

$212uf$

Therefore a capacitor of $2200uF$ capacitance was chosen

2.1.2 The Rectifier (Bridge) Wo1

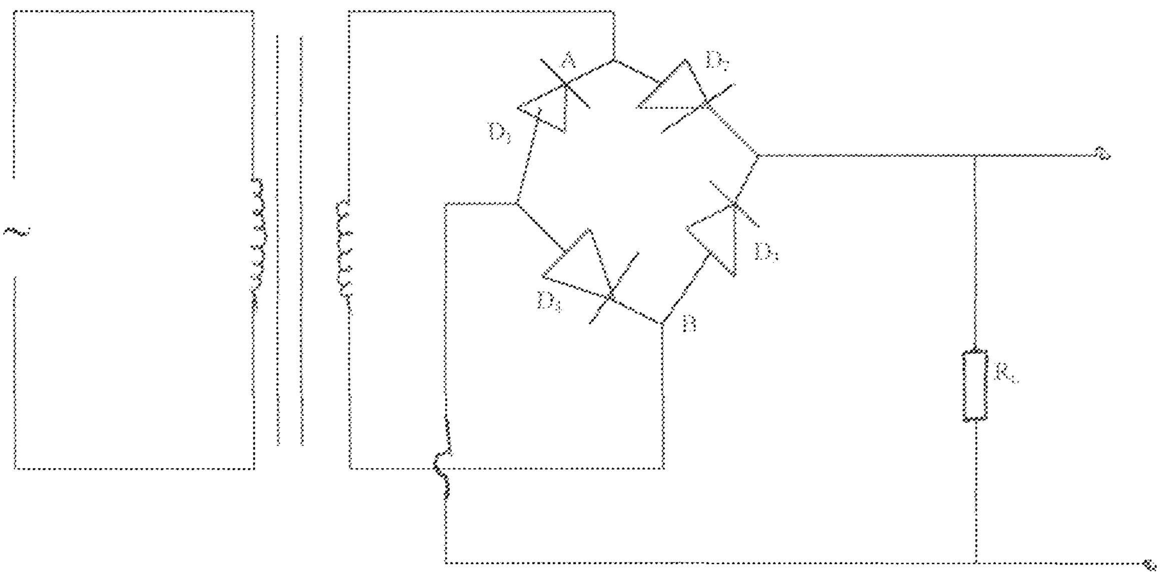


Figure 3.

A rectifier is the arrangement of diode(s) to convert Ac voltage to a pulsating Dc voltage. For analysis, we shall limit our scope to the full-wave bridge type of rectifier. The full wave bridge uses four diodes arranged in bridge shown as in fig. 3.

During the half cycle of the input at point A positive w.r.t. B: diodes D_2 and D_4 conducts. Current therefore flows. During the other half cycle, that is point A is negative w.r.t B: D_1 and D_3 conducts while D_2 and D_4 blocks. Current flow from B to A through D_3, R_L and D_1. Both current passes through the load, R_L, in the same direction and so a fluctuating un-directional voltage is developed across the load having the wave form as shown in fig 3.1

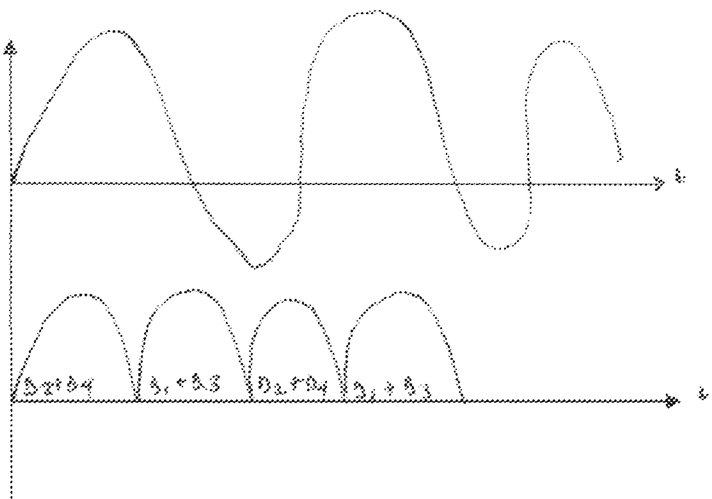


Figure 3.1

In considering rectifiers for design purposes, it is always important to know the peak voltage, PIV that appears across the diodes. The PIV of a full wave bridge type is twice the maximum voltage.

$$Vrms = \frac{Vmax}{\sqrt{2}}$$

$$= \frac{1}{\sqrt{2}} x \ Vmax = 0.707Vmax.$$

$$Vdc = \frac{2Vmax}{\pi} = 0.636Vmax$$

PIV = 2Vmax

The Bridge Rectifier used has the following rating :-

Maximum input V = 70V

Maximum Capacitance = $2500uF$.

Maximum Voltage per diode = 1.1V @ 1A

2.1.3 IC Regulators.

Integrated – circuit voltage regulators provide the benefits of low cost, small size and high performance. They are normally used to regulate supply voltages locally on each individual circuit board of a large system. A wide range of types are available as either fixed voltage (three-terminal) or variable voltage (four-terminal) in which the fourth lead is used as the 'control' terminal. A typical fixed-voltage regulator is the 7805V regulator, which is easily used as shown in fig 2.1

More complex forms such as switching regulators are quite common owing to their flexibility in application and their ability to provide good regulation at low cost.

Fore the purpose of the this project the type of IC regulator used are 7805 and 7905 and the both IC has the following characteristics:-

For 7805:

Output Imax = 1A
Output V = + 5 $\pm$ 4%

Quiescent I = 4.2MA

For 7905

Output Imax = 1A

Output V = - 5 ± 4%

Quiescent I = 1MA.

2.1.4 A. C Filtering / Smoothening

A half or full wave rectified-voltage wave form may be smoothed out to provide an approximate d.c voltage using a capacitor shunted across the load to act as a filter. The capacitor stores energy during the conducting period and delivers this energy to the load during the non-conducting period. The deviation of the load voltage from it average or d.c. value is referred to as the ripple voltage.

Referring to fig 4 which show the half-wave rectifier circuit with capacitor smoothing and the associated output voltage and diode current wave forms, the following simplifying approximation are made:-

a. The load-time constant CR_L is large compared with the period of the rectifier output wave form, so that the charging interval θc is small compared with the cycle time T.

b. The diode current id is assumed to be triangular.

c. The diode switching time α_2 when the capacitor is fully charged occurs at the peak of the supply voltage (i.e. at wt = $^{\pi}/_{2}$)

d. The sinusoidal and exponential parts of the output voltage can be approximate by straight lines.

e. The source impedance is negligible.

f. The forward voltage across a conducting diode is assumed constant, irrespective of currents.

Considering the waveforms, for half-wave rectifier shown in fig 4a1

$$Vdc \approx Vm - \frac{Vr}{2}$$

and

$$Sin\,\alpha_1 = \frac{Vm - Vr}{Vm}$$

$$\therefore \alpha_1 = \sin^{-1}\left(\frac{Vm - Vr}{Vm}\right)$$

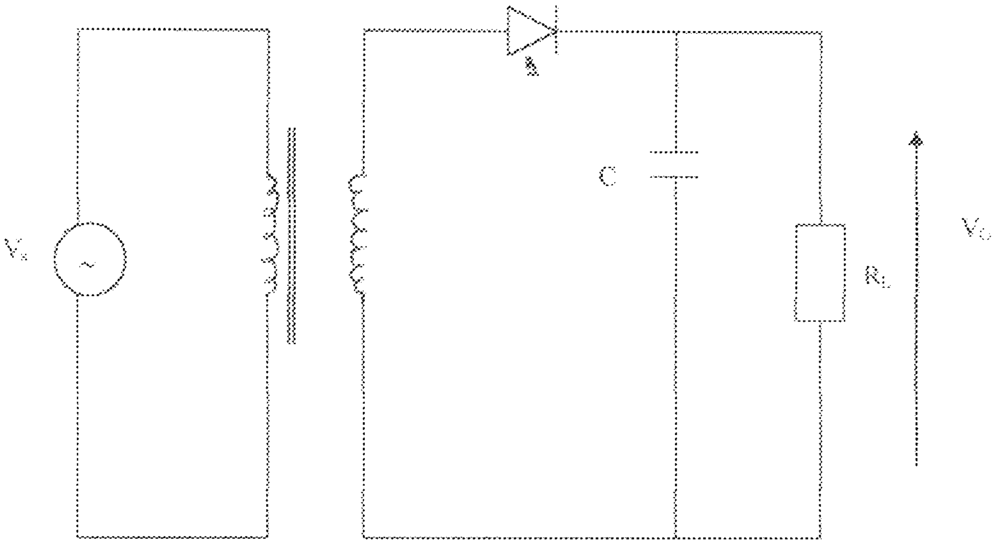


Figure 4

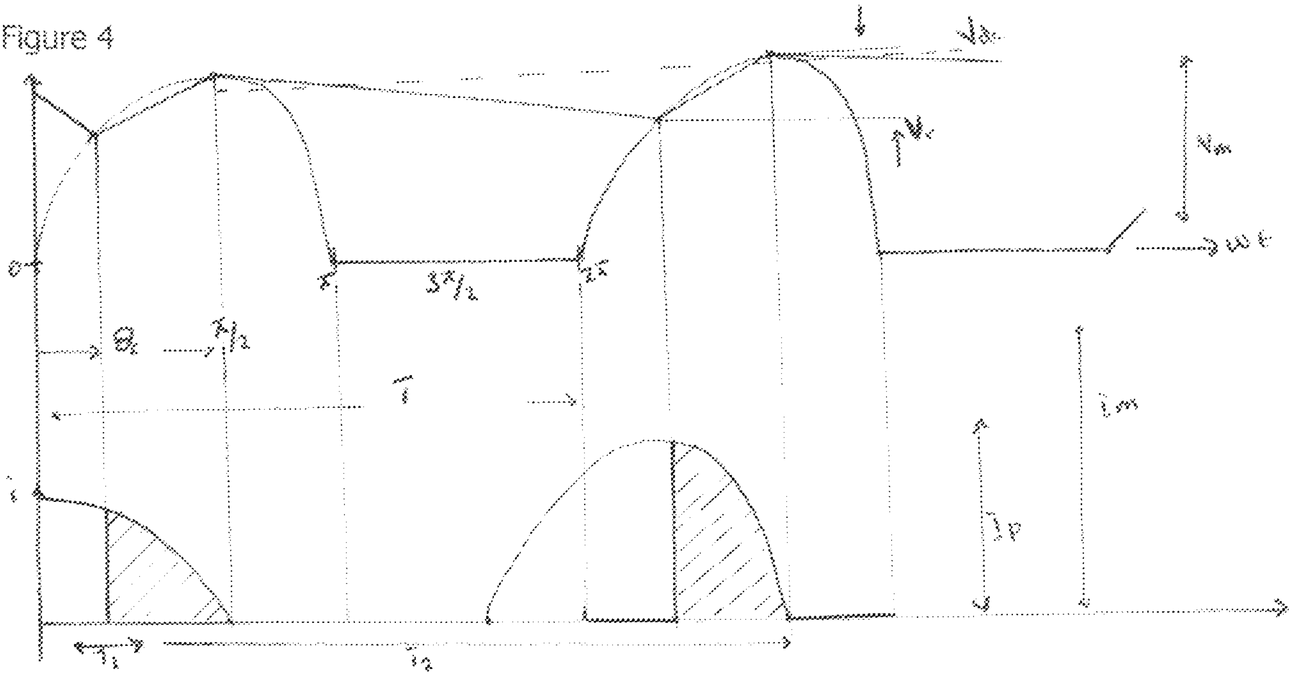


Figure 4.1 Half-wave rectifier with capacitor smoothing.

But $\alpha_2 = {}^1/_2\pi$

$\therefore \theta_c = \alpha_2 - \alpha_1 = {}^1/_2\pi - \text{Sin}^{-1} \left(\frac{Vm - Vr}{Vm}\right)$

or $\cos\theta_c = \left(\frac{Vm - Vr}{Vm}\right)$

During the charging period, the accumulated in the capacitor C is given by Q = CV_r.

This charge is transferred to the load during discharge, the charge lost by the capacitor being given approximately by:

$Q = Idct,$

Since $T_2 \approx T,$

$\therefore I\,dc\,T = CVr$

$\therefore V_r = \left(\frac{IdcT}{C}\right)$

but $T = \left(\frac{1}{fc}\right)$

$\therefore V_r = \left(\frac{Idc}{fc}\right)$

and Vdc = $IdcR_L = fCR_LVr$.

The ripple factor γ is given by

γ = r.m.s value of all a.c components / d.c component

Since we have assumed that the ripple has a triangular wave-form of peak value Vr/2, its r.m.s value can be shown to be

$$\frac{Vr}{2} x \frac{1}{\sqrt{3}}$$

$$r = \frac{Vr}{2\sqrt{3}Vdc}$$

For the full - wave coase, the wave form period is half that for the half - wave.

$$\therefore T_2 = \frac{1}{2f}$$

$$Vr \approx \frac{Idc}{2fc}$$

2.2.1 *Transmitter*

The output of the oscillator is fed into the input of the transmitter. Q_1 serves as a switch. The transistors Q_2 and Q_3 are connected as emitter follower, acting as a buffer for the driving of infrared and LED they both operate at a frequency 36.7KHz. the overall gain is given by:

$Av = Av_1 Av_2$

From data book Q_2 hfe = 350 and Q_3hfe = 25

At 100mA the gain is given as:-

$Av = 350 \times 25$

$Av = 8750$

Q_1 = Bc 557, Q_2 = Bc337, Q_3 = Tip31

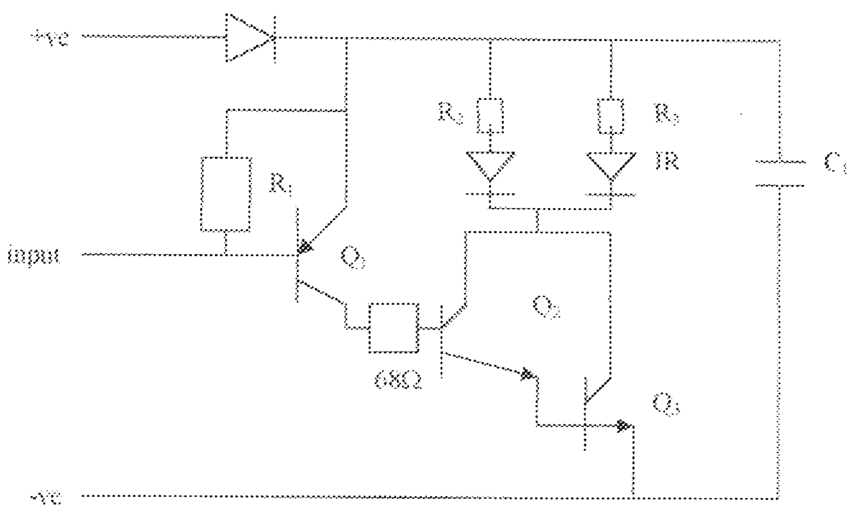


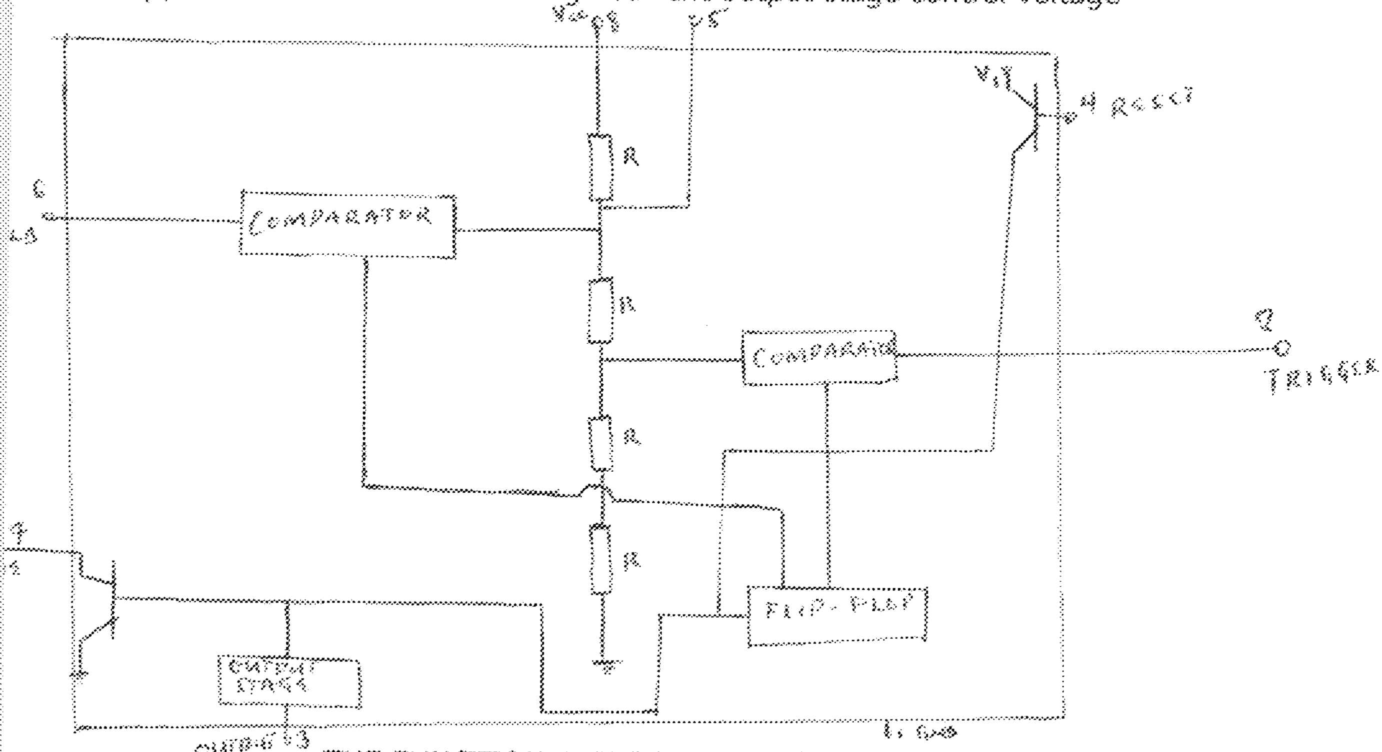
Figure 5.8

2.2.3 Oscillator

Monolithic integrated circuit timers have a wide range of application in linear and digit circuitry. In many cases these circuits are a direct economical replacement for mechanical and electron-mechanical timing devices.

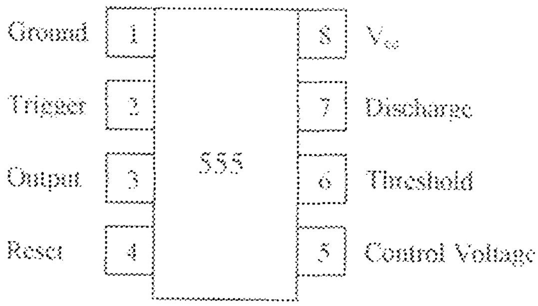
The most popular of the present Ic timers is the 555, which is available in an 8-pin duct-in-line (Dib) package in both bipolar and CMOS forms. Additionally a 14-pin package containing two 555 timer may be used: this is generally designated as the 556 timer although number designations do vary with manufacturer. The 555 timer is basically a very stable is capable of being operated either as an accurate bistable, monostable or astable multivibrator.

The timer comprises 23 transistor, 2diodes and 16 resistors. The functional block diagram is shown in figure 5.1 and consist of two comparator, a flip-flop, two control transit and a high current output stage control voltage



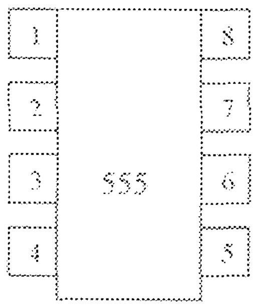
THE FUNCTIONAL BLOCKED DIAGRAM OF 555 TIMER

The comparators are actually operational amplifier that compare input voltage to internal reference voltages which are generated by an internal voltage divider chain of three 500Ωresistors. The reference voltages provided are one – third of V_{cc} and two thirds of V_{cc}. When the input voltage to either of the comparator is higher than the reference voltage for that comparator, the amplifier goes into saturation and produces an output signal to trigger the slip-flop. The output of the flip-flop controls the output state of the timer. The pin out connection for the 555 timer are shown in fig 5.1



(a) Top View

Bipolar pin-out-diagram



(b) Top view

C-Mos pin-out-diagrams

For the purpose of this project. Astable multivibrator is used. To achieve the astabel circuit we made use of the monostable circuit but split the timing resistor into two separate values R_1 and R_2 with their junction connected to pin 7. pin 2 and 6 are connected, just as in the previous circuit, to provide continuous triggering. With power applied trigger and threshold input are both below Vcc/3V and the timing capacitor is uncharged. The output voltage is high and stays high for a period given by:

T_1 = 1.IC (R_1 + R_2) seconds which is the initial charging time taken by capacitor C to reach the upper threshold value of $2V_{cc}/3$. The upper comparator will trigger the flip-flop and the capacitor will being to discharge through resistor R_2. This takes a time of t_2 0.693CR_2 seconds just as before, since the lower threshold level aimed at is $V_{cc}/3$. The timer now retrigger itself and C begins to recharge. Not, however, that the time now taken to reach the upper threshold level is $0.693C(R_1 + R_2)$ since the charging cycle is started from Vcc/3 and not OV as was the initial case. All charging cycle times will have this value apart from the initial one. Thus the total time required to complete a charge and is charge cycle is

$t = t_1 + t_2 = 0.693C(R_1 + 2R_2)$ seconds.

and the frequency of oscillation is $^1/_T$ so that

$$f = \frac{1.44}{C(R_1 + 2R_2)} \text{ Hz}$$

As R_2, the circuit of this astable is shown is figure 5.2

The duty cycle defined as the on time as a percentage of the total cycle time, is given is this case by the ratio

$$\frac{R_2}{R_1 + 2R_2}$$

As r_2 decreases the duty cycle approaches zero and R_2 increases the duty cycle approaches 50%

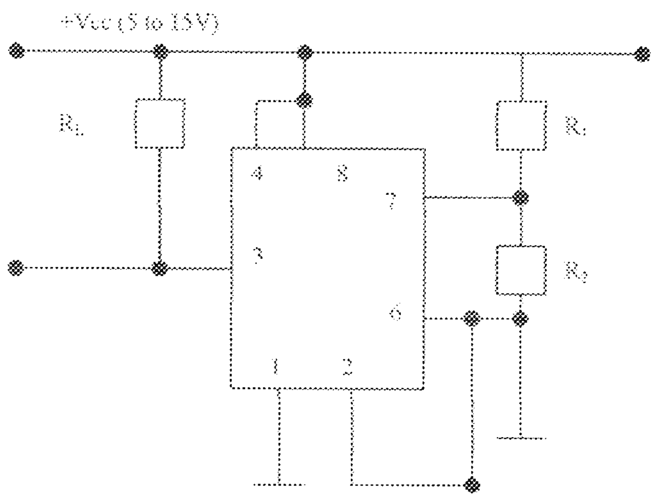


Figure 5.2

2.2.4 Amplifier.

For the purpose of this project the Darlington connection was used to amplifier the signal. If you hook two transistors together as in figure 6, the result behaves like a single transistor with beta equal to the product of the transistor betas. This can be very handy where high currents are involved (e.g. voltage-regulators or power amplifier output stages), or for input stages of amplifiers where very high input impedence is necessary.

For a Darlington transistor the base-emitter drop is twice normal and the saturation voltage is at least one diode drop (since Q_1's emitter must be a diode drop above Q_2's emitter). Also, the combination tends to act like a rather slow transistor because Q_1 cannot turn off Q_2 quickly. This problem is usually taken care of by including a resistor from base to emitter of Q_2 (fig 6.1) R also prevents leakage current through Q_1 from biasing Q_2 into conclusion; its value is chosen so that Q_1's leakage current (nanoamps for small-signal transistors, as much as hundreds of microamps for power transistors) produces less than a diode drop across R and so that R doesn't sink a large proportion of Q_2's base current when it has a diode drop across it. Typically r might be a few hundred ohms in a power transistor Darlington, or a few thousand ohms for a small-signal Darlington.

Darlington transistor are available as single packages, usually with the base-emitter resistor included. A typical example is the npn-power Darlington 2N6282, with current gain of 2400 (typically) at a collector current of 10amps.

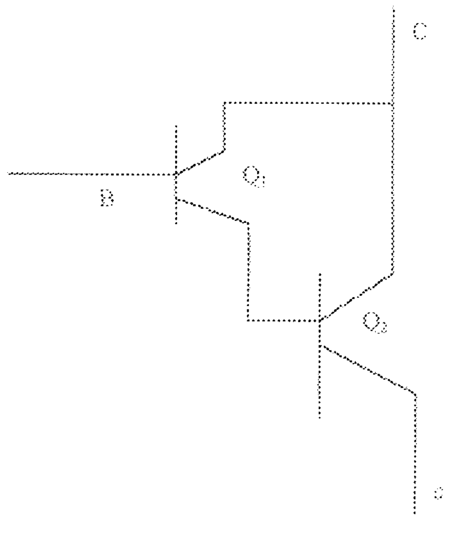


Figure 6.0 Darlington Transistor Configuration

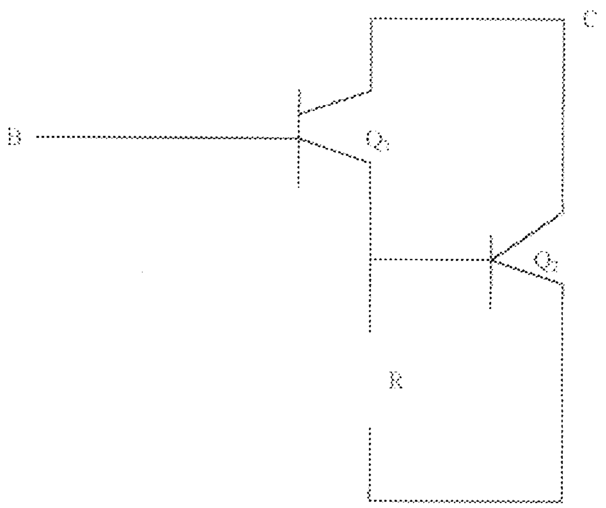


Figure 6.1 Improving turn-off speed in a Darlington pair.

2.2.5 The Infra-Red Emitter: this is a solid state gallium arsenide that emits a beam of radiant flux when forward biased. When forward biased, electrons from the n-region will recombine with excess holes of the p-material in a specially designed recombination region sandwiched between the P and n-type material. During this recombination process, energy is radiated away from the device in the form of photons. The generated photons will either be reabsorbed in the structure or leave the surface of the device as radiant energy. A few areas of application for such devices include card and paper tape reader, shaft encoders, data transmission system.

2.2.2.1 Infrared receiver

The receiver circuit shown in figure is divided into infrared receiver, the amplification, wave shaping and switching or pulse generation. When infrared signals fall on the infrared diode the potential at the PN-junction is reduced to almost zero, hence current flow from via to ground being connected in a voltage divider network with negligible resistance, only about 0.7V is dropped on the diode. The infrared signals are received as pulses. The resistor R_1 serve as a current limiting resistor which avoid damage to the infrared diode hence allow a current or only $\frac{9}{1x10^6}A$ i.e. 0.009MA to flow across the diode.

2.2.2.2 Amplification

The second stage is the two stage collector base biase amplifier which amplifies the input voltage i.e. the voltage across the infrared this is coupled via the capacitor C_1. The transistor used is BC/09 with life = 520. The first

V_{in} when infrared signals falls on diode is 0.6V

Current $\frac{9}{1x10^{6}} = 0.009MA$

Stage 2:

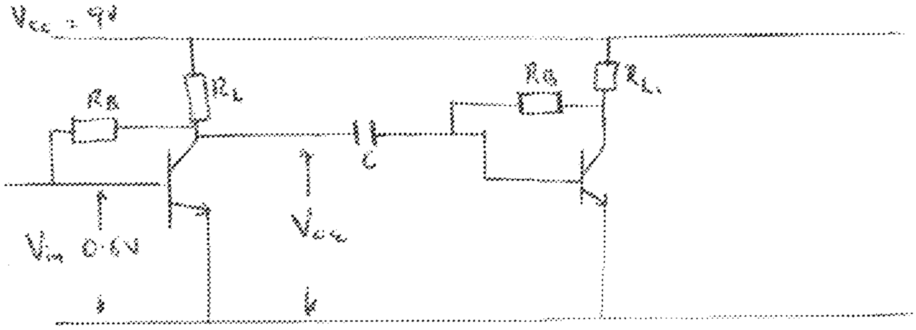


Figure 7.2

At each stage.

$V_{cc} = I_C R_L + Vce$.........................(i)

$V_{cc} = I_B R_B + V_{BE}$........................(ii)

$I_c = 520 I_B = \frac{I_C}{I_B} = 520$

Where BC 109 hfe = 520

$V_{cc} = I_B \times 3.3 \times 10^6 + 0.6$

$\frac{I_c}{520} = 3.3 \times 10^6 + 0.6$

$I_c 6.346 \times 10^3 + 0.6$................(3)

Substituting equation (3) in equation (1)

$V_{cc} = I_c \times 4.7 \times 10^3 + 6.346 \times 10^3 I_c + 0.6$

Where V_{cc} = 9V.

$9 = 4.7 \times 10^3 I_c + 6.346 \times 10^3 I_c + 0.6$

$9 - 0.6 = 11.046 \times 10^3 I_c$

$I_c = \frac{8.4}{11.046. \times 10^3} = 760 \times 10^{-6}$

$\approx 0.76MA$

$I_B = \frac{I_c}{520} = 1.462 \times 10^{-6}$

$= 0.0015MA$

$V_{ce} = I_B R_B + V_{Be} = 5.55V$

For stage 4

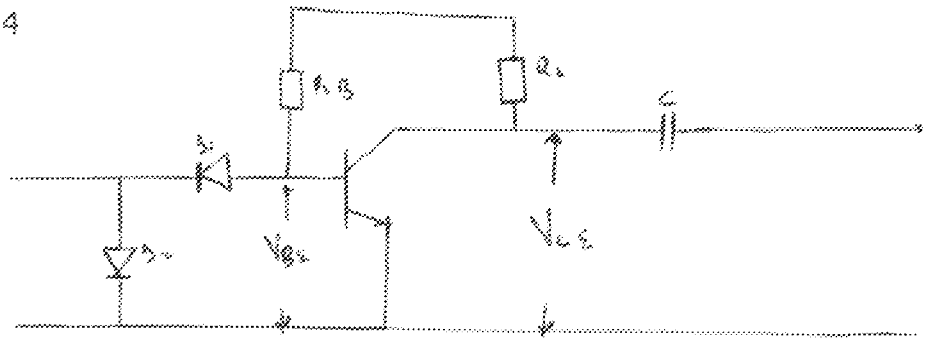


Figure 7.3

$R_B = 470k\Omega$ R_L $4.7k\Omega$

$V_{cc} = I_B R_B + V_{BE}$ ....(i)

$V_{cc} = I_C R_L + V_{CE}$...................(2)

$I_B R_B + V_{BE} = I_C R_L + V_{CE}$

$I_B \times 470 \times 10^3 + 0.6 = I_C \times 4.7 \times 10^3 + V_{CE}$

$I_B \times 470 \times 10^3 + 0.6 = 520\ I_B \times 4.7 \times 10^3 + V_{CE}$

$I_B (47 \times 10^3 - 520 \times 4.7 \times 10^3) = V_{CE} - 0.6$

$- I_B \times 1.974 \times 10^6 = V_{CE} - 0.6$

$-1.974 \times 10^6 I_B = V_{CE} - 0.6$

where $V_{CE} = 4.5V$.

$-1.974 \times 10^6 I_B = 4.5 - 0.6$

$$I_B = \frac{3.9}{1.974.10^6} = \frac{3.9 \times 10^6}{1.97}$$

$= 1.9797 \times 10^{-6}$

$= -1.98 \times 10^{-6}A$

$= - 0.00198MA.$

2.2.2.5 Counter

The type of counter used for this project is the Asynchronous counters. A commercially available four-stage pure binary counter (÷6) is the 7493. the circuit is internally divided into a ÷2 and ÷8 section. The circuit arrangement is shown in fig 8. This circuit can function as pure binary -16 counter by taking the input pulses to be counted to pin 14 (input A) and making an external connection between pin 12 (Q_A) and pin 1 (B input). The reset inputs are not required so should be earthed.

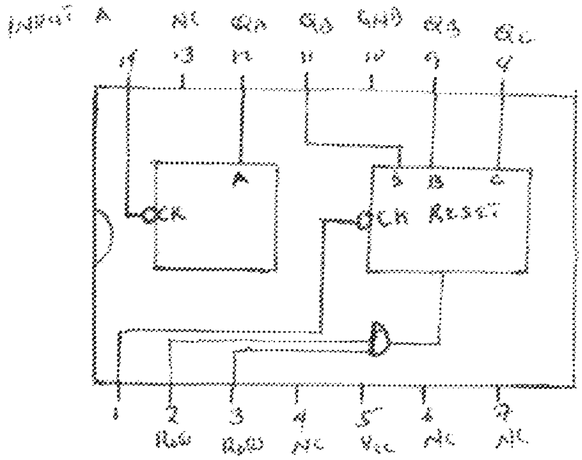


Figure 8 SN7493 pure binary madulo 16 counter package

A modified count can easily be produced using the reset method by using the reset input. For example the circuit of fig. 8.1 will produce a ÷11 count. Here Q_D is connected directly to $R_{0(2)}$ and the output of an AND gate, whose inputs are Q_A and Q_B, is connected to $R_{0(1)}$. The count Df 11 is only value between 0 and 11 where Q_D =1 and $Q_A.Q_B$ =1 so that a result is produced after the binary equivalent of decimal 11 has appeared on the output lines for a short period.

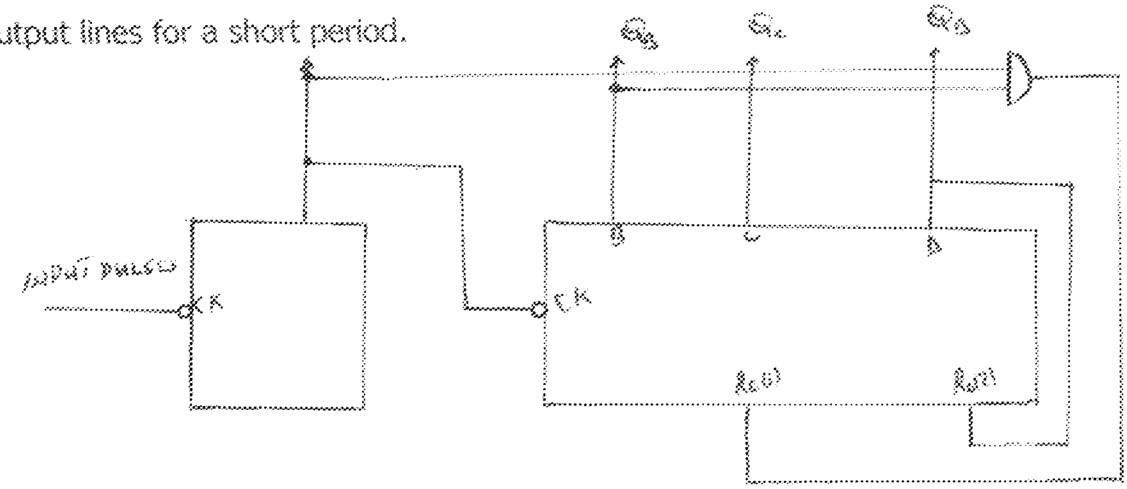


Figure 8.1

2.2.2.6 BCD to Decimal Decoder

The 4028Ic is a BCD decimal or binary-to-octal decoder. It consists of four inputs, decoding logic gates and 10output buffers. A BCD code applied to the four input A, B, C and D results in a high level at the selected 1-of-10 decimal decoded in outputs. Simply, a 3-bit binary code A,B and C is decoded in octal at output 0-7. A high level signal at the D input inhibits octal decoding and causes output 0-7 to go low. All inputs are protected against static discharge damage by diode damps to VDD and Vss.

The k has a propagation delay of 300ns at 5v, 130ns at 10v and 90ns at 15v. Both inputs and outputs are Buffered and can be used as a 3-8 line decoder.

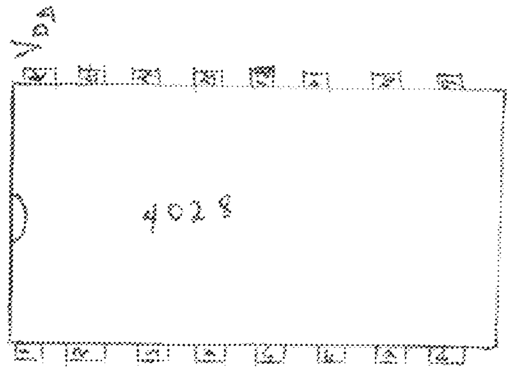


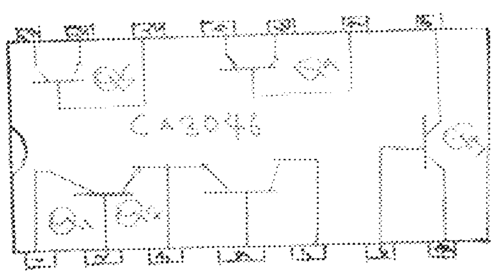
Fig. 9 A BCD to decimal decoder (4028)

2.2.2.7 *Transistor Array*

The C_A3046 consist of five silicon NPN transistor on common..............substrate in a 14 – lead dual in line plastic package. Two transistors are internally connected to form a differential amplifier. The transistor of the C_A 3046 well suited to low noise general purpose and to a wide variety of applications in addition they provide the very significant inherent integral circuit advantages of close electric and thermal matching.

Each transistor has a rating of V_{CE}, 15V, V_{CBO} 20v, V_{EBO} 5V, I_C 50MA, power dissipation 300mW and 750mw for the whole package.

Fig 10



2.2.2.8 Attenuation for the Variable Resistor.

The variable resistor is 250k this is replaced with 10 resistor each of 50kΩ x 2, and 20kΩ x 6.

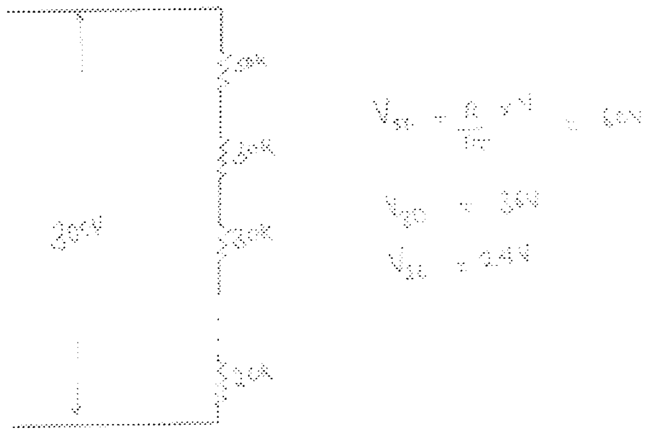


Fig 11
~~Diagram~~

2.3 Dimmer Circuit

2.3.1 S.C.R.S

S.C.R.S and trials are members of the thyristor family. They act as high speed power switches. They are solid-state devices and can operate at potentials up to several hundred volts and can handle current up to tens or hundreds of amps. They can be used to replace conventional mechanical-switches and relays in many d.c. and a.c power control systems and can readily be used to control electric lamps, motors, heaters and alarms.

The S. C. R. or Silicon Controlled Rectifier, is a four-layer pnpn silicon semiconductor device and is represented by the symbol shown in figure 12. Note that this symbol resembles that of a normal rectifier, but has an additional terminal known as the 'gate.' The S.C.R. can be made to act as either an open-circuit switch or as a silicon rectifier, depending on how its gate is used.

2.3.3 Phase Triggering Circuit

Figure 14 shows the basic phase-triggered circuit, using a trial as the power control element. The load is wired in series with the triac and the combination is connected across the a.c power line. The trial gate-trigger signal is derived from MT_2 via a variable phase-delay network and a trigger-device. The phase-delay network enables a.c. voltage to the input of the trigger device to be delayed to that on MT_2 by an amount fully variable from (ideally) $0°$ to 180^0, i.e., by as much as one half-cycle of line voltage.

The trigger device is a voltage-operated 'switch' that triggers on and fires the triac when a preset voltage is reached at output of the phase-delay network or at the end of the pre-set phase-delay period.

Figure 14.1 shows the wave-form that occurs in different sittings of phase delay. Thus, if the phase delay network is set for only a 10^0 delay the triac is triggered on 10^0 after the start of each half-cycle, and then self-latches and stays on for the remaining 170^0 of each half-cycle. Almost the full available line power is thus applied to the load under this condition.

If the circuit is set for a phase-delay of 90^0, the triac does not turn on until half-way through each half-cycle, and only half of the maximum possible power is applied to the load. Finally, if the circuit is set for a 170^0 delay the triac does not turn on until 10^0 before the end of each half-cycle and very little power is applied to the load under this condition. Thus, the load power can be varied all the way from zero to maximum by varying the setting of phase-delay control. Since the triac is either fully off or is saturated at all

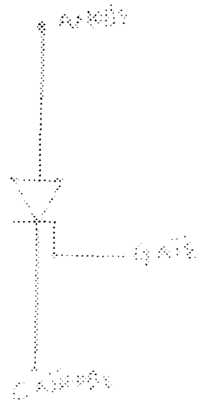


Fig. 12

2.3.2 Zero – Crossing Detector

The circuit shown in fig 13 generates an output square wave for use with TTL logic (zero to – to 5v range) from an input wave of any amplitude up to 100volts R_v combined with D_1 and D_2, limits the input swing to – 0.6volt to +5.6volts, approximately. Resistive divider R_2R_3 is necessary to limit negative swing to less than 0.3volt, the limit for a 393 comparator. R_3 and R_6 provide hysteresis, with R_4 setting the trigger points symmetrically about ground. The input impedance is nearly constant, because of the large R_1 value relative to other resistors in the input attenuator. A 393 is used because its inputs can go all the way to ground, making single supply operation simple.

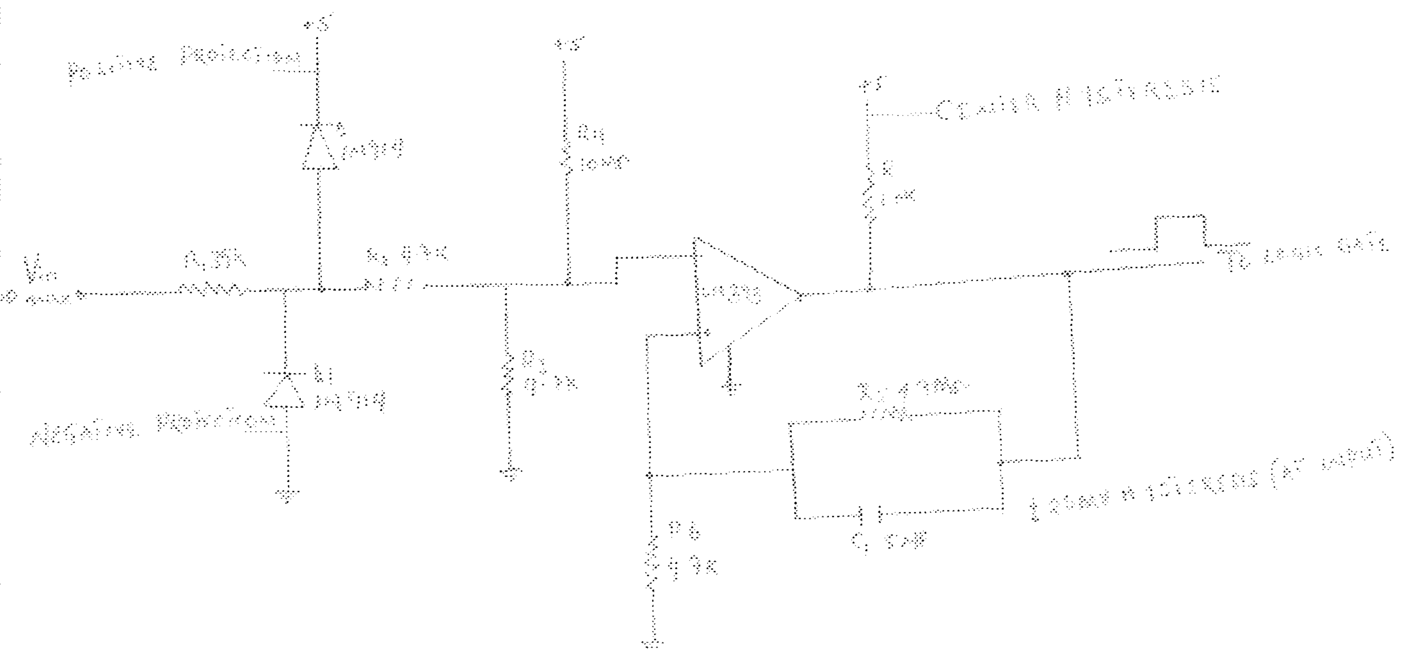


Fig. 13 ZERO CROSSING LEVEL DETECTOR WITH INPUT PROTECTION.

times very little power is 'lost' in the device and very efficient variable power control is obtained.

The actual phase-delay section of figure 1.1 circuit can take either of two basic forms. It can consist of either a single or multiple R-C variable phase shift network or an R-C variable time-delay network.

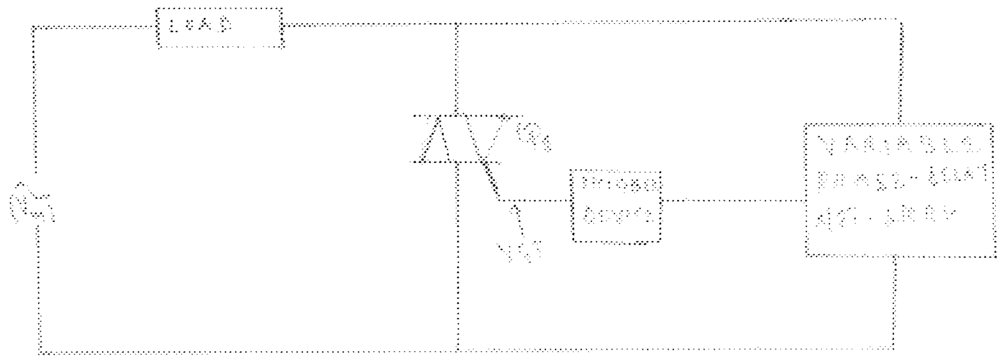


Fig. 14 BASIC PHASE-TRIGGERED VARIABLE POWER-CONTROL CIRCUIT

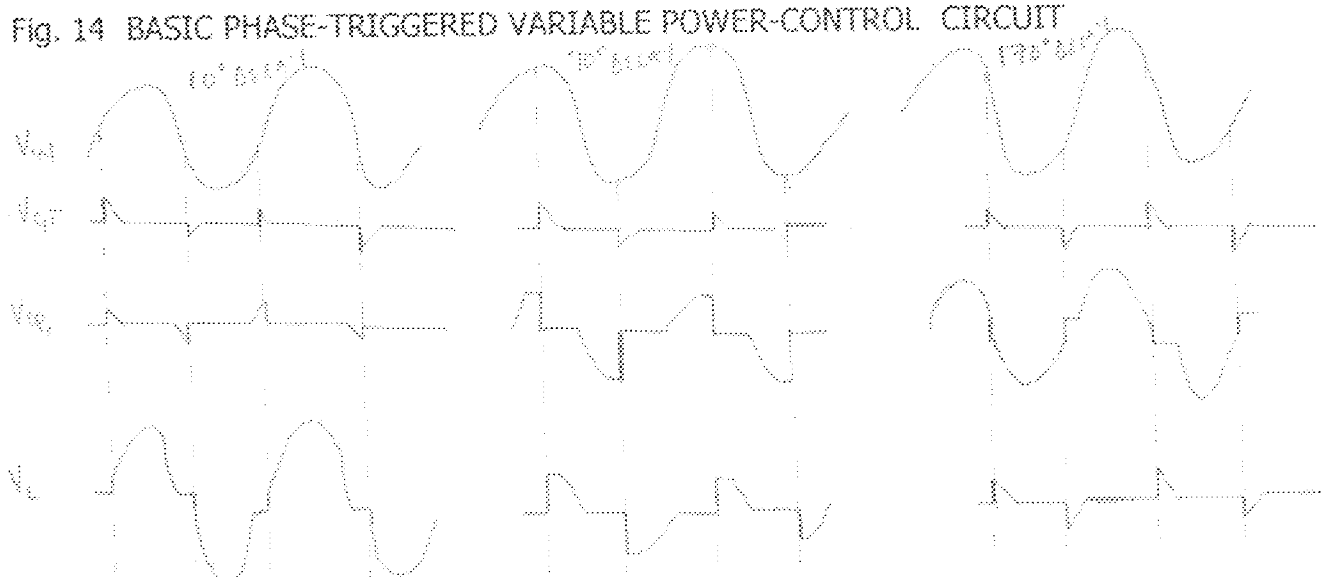


Fig. 14.1 WAVEFORMS OF FIG 14 CIRCUIT AT VARIOUS PHGASE-DELAY SETTINGS.

2.3.4 Radio – Frequency Interference (r.f.i)

When S.C.R.S and triacs are used to switch power into a load these high switching speed result in the generation of a series of harmonically related radio-frequency signals. The magnitude of the device switching current and may be so great that it causes interference on a.m. radios.

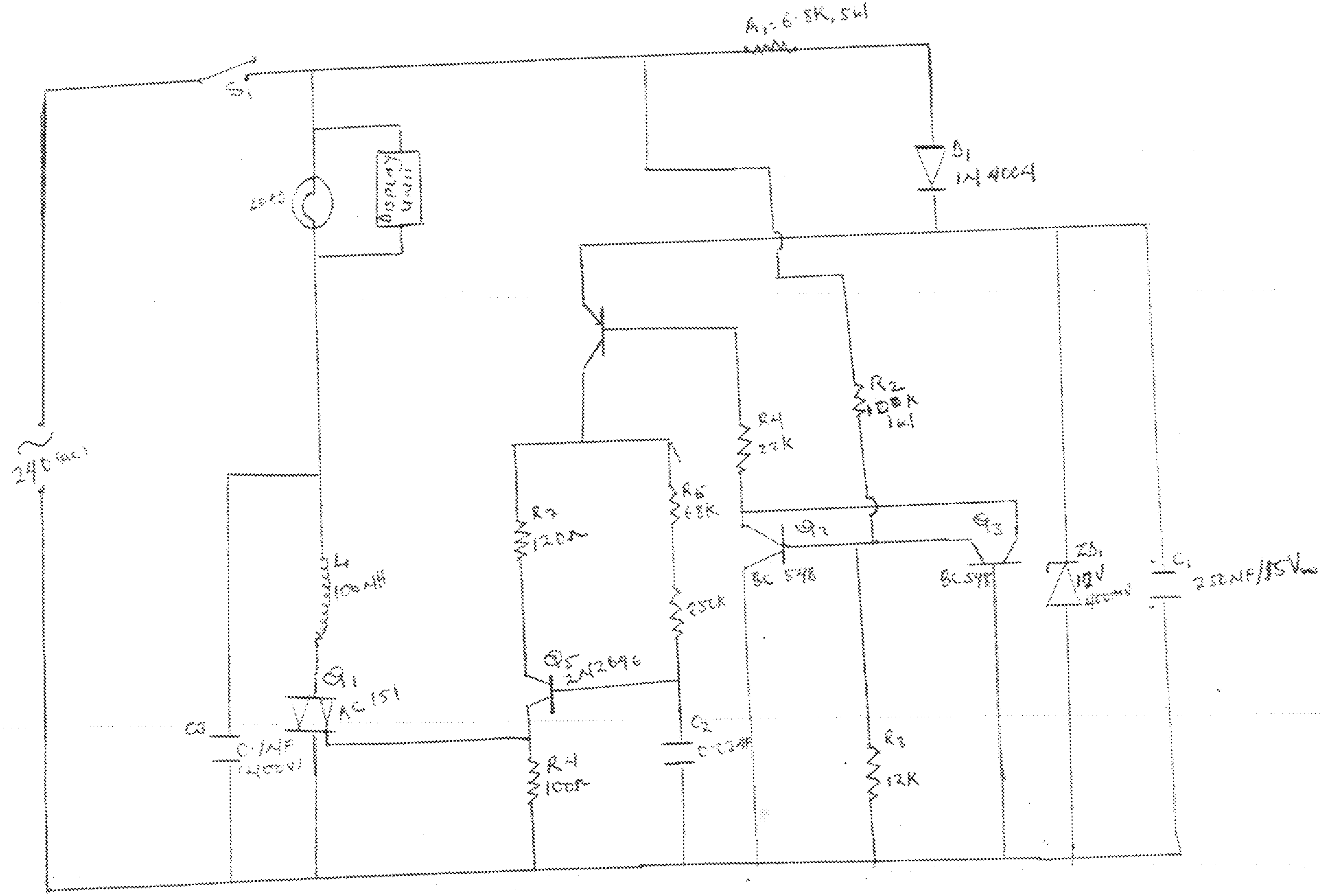


Fig 14·2 DIMMER CIRCUIT.

Two basic types of radio-frequency interferences (r.f.i) may be generated by S.C.R.S and triacs when they are used in line-powered switching applications. One of these is radiated radio-frequency interference (r.f.i) which is radiated directly into the air as a radio signal. In most cases this type of radio-frequency interference is of such low intensity that it does not cause significant interference with a.m. radio unless they are placed very close to the source of radiation. If radiated radio-frequency is troublesome, it can be minimized by mounting the thyristor circuitry in a screened container.

The second and more troublesome type of radio-frequency interference is conducted radio-frequency interference which is carried through the power lines and may affect radio and Tv sets connected to the same power lines. Trouble from this type of radio-frequency interference can be minimized by connecting a simple L.C filter in series with the power-line, so that the conducted high-frequency harmonics of the basic switching signal are reduced to significant level.

2.4.0 Display Circuit

2.4.1 Attenuation

The IC 7107 is connected in the 2V display made. The precision rectifier is fed with 1V and the output varied through a variable resistor between 0 and 2V. The 300Vac from the dimmer circuit must be attenuated; this is done through a voltage divider network at a ratio of 300V:1V for the mains voltage to precision amplifier input respectively. The figure 15 below shows the voltage divider network.

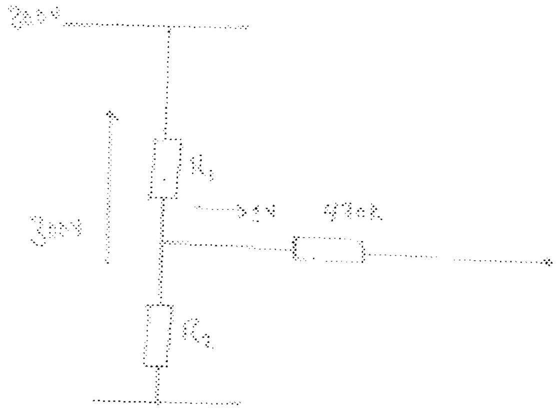


Figure 15

Current across R_1 & R_2 is the same.

Where $V_1 = 1V$

$R_1 = 15m\Omega$

Using voltage divider,

$$V_1 = \frac{R_2}{R_1 + R_2} \times 300$$

$$1 = \frac{R_2}{15 \times 10^6 + R_2} \times 300$$

$$15 \times 10^6 \times R_2 = 300R_2$$

$$15 \times 10^6 = 299R_2$$

$$R_2 = \frac{15 \times 10^6}{299} = 50k\Omega$$

$$\therefore R_2 = 50\Omega$$

2.4.2 Precision Amplifier:

The precision amplifier is of the two that is

(a) The precision half wave rectifier &

(b) The precision full wave rectifier

For the purpose of this project the precision full wave rectifier was used.

ii. The Precision Full Wave Rectifier.

The half-wave circuit can be adapted in various ways to provide precision full-wave rectification. A common form is shown in fig 5.198. Amplifier A, provides half-wave rectification blocking the negative half-cycles of the input and inverting the positive half-cycles with a gain of unity. Amplifier a_2 is a summing inverting amplifier with a gain of -1 for input signal V_1 and gain of -2 for the rectified output V_{01}. The waveforms are shown in figure 16. Wave forms (c) and (d) show the output of A_2 resulting from the two inputs taken separately. Output (c) would be that if R_4 was opened while output (d) would result if R_5 was opened. The total output (e), is the sum of the other two precision rectifications requires tight tolerance resistor for R_1, R_2, and R_5. If an average of d.c output is required, the INF capacitor shown can be added to the circuit converting A_2 into a summing integrator.

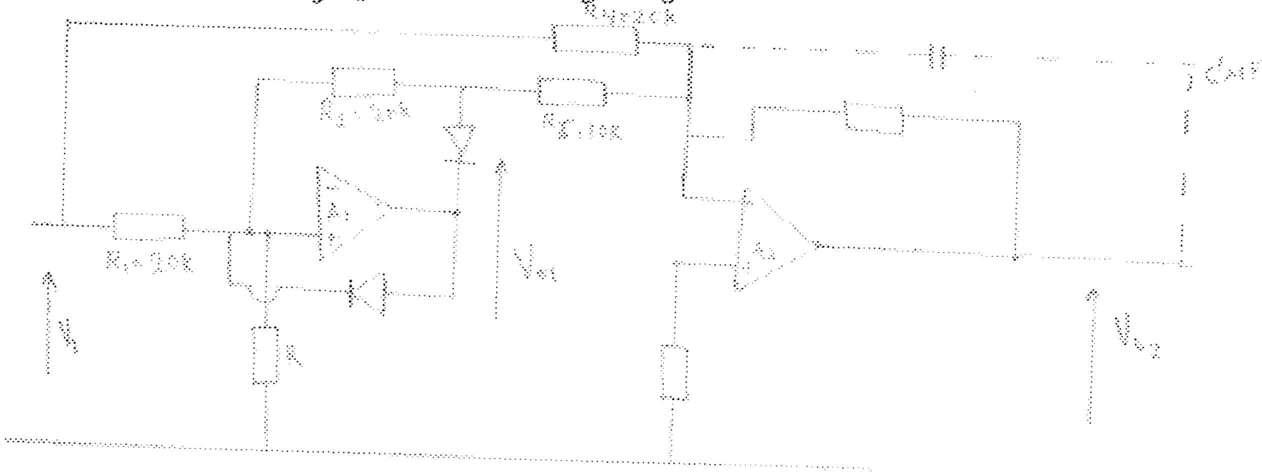


Figure 16 THE PRECISION FULWAVE RECTIFIER

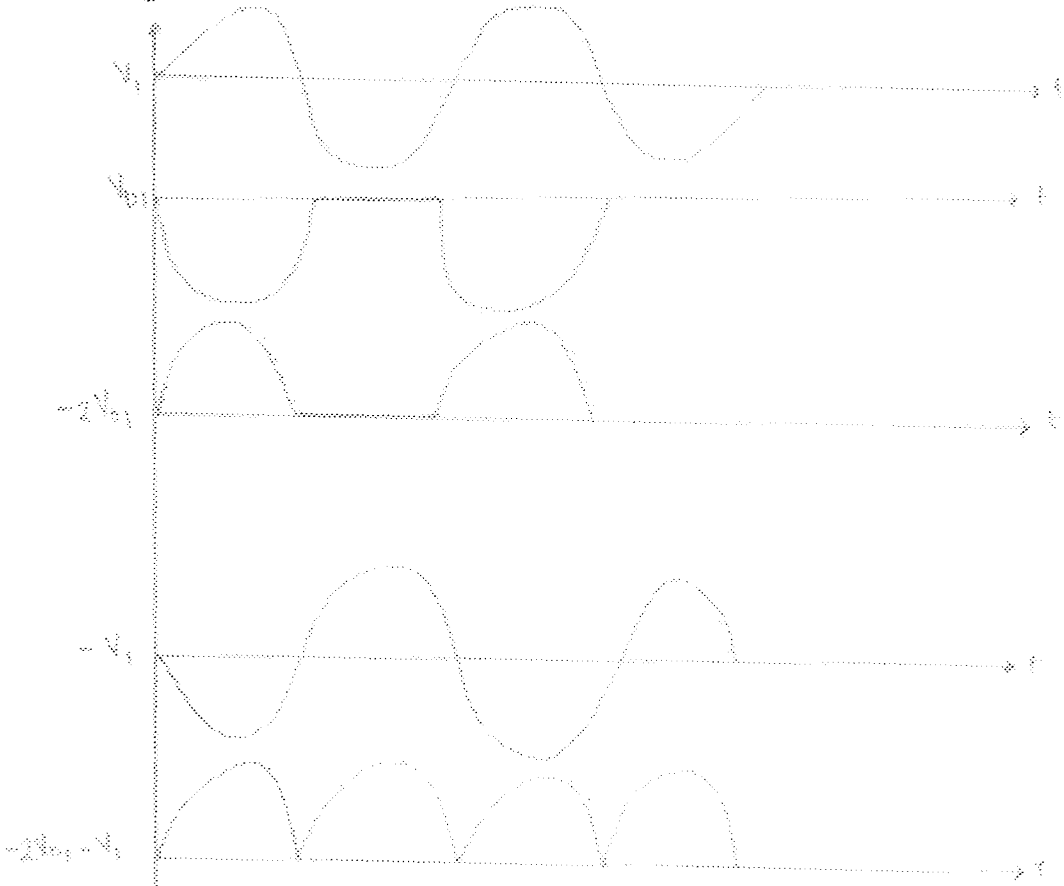


Figure 16.1 WAVEFORMS FOR THE PRECISION FULL-WAVE RECTIFIER

2.4.3 Analog-to-digital (A/D)Converter:-

Figure 17 shows a schematic for complete $3^1/_3$ digit A/D converter using an intersil ICL 7107CPL. This IC chip is chosen because it digitizes both positive and negative voltages and requires a minimum of external components. It is also designed to drive common-anode LED display directly. This IC chip employed dual-slope conversion technique which has employed dual-slope conversion technique which has being fully described in section. The ICL 7107CPL comprises of both analog and digital parts. The digital part consists mostly of a decade counter-latch-display module. The LED displays are driven directly rather than multiplexed. This eliminates nay switching noise that would be produced on the V_{cc} line by digits being turned on and off during multiplexing. The LED segment currents are internally limited to about 8mA, so no external current-limiting resistors are needed. The circuitry that controls the integrator and an oscillator which produces the basic clock for the converter is also part of this section. The frequency of the clock is determined by the value of resistor R and the capacitor C connected between pins 38 and 39 respectively. Analog part consist of an integrator, a comparator and MOS switches which are used to determine which signal is applied to the input of the integrator and other parts of the circuit at various times in the conversion cycle. A conversion cycle for this converter is divided into four periods rather than two as described for basic dual-slope converter. The two additional periods or phases allow the converter to work with both positive and negative input voltages and cancel out the effect of off-set voltages in the internal circuitry.

Mode of Operation:-

During the auto-zero phase, the reference capacitor (ref is charged to a voltage equal to the reference voltage. Charging the reference capacitor to the reference voltage allow the converter to work with both positive and negative voltages. Auto-zero capacitor C_{AZ}, is equally charged to a voltage equal to the sum of the off set voltages in the buffer amplifier-integrator and capacitor. This will cancel out the effects of any offset in the circuit. This is followed by the signal integrate phase. In this phase, the differential voltage between the input high (INH_1) and the input LOW (INLO) pins is applied to the input of the integrator for 1000 clock cycles.

For a positive input voltage, the integrator output will ramp down and for a negative input voltage, the integrator will ramp up. The polarity flip-flop will be set or reset to show which way the integrator output ramped. The reference integrate phase forms the third phase of the conversion cycle.

Depending on the setting of the polarity flip-flop, the reference capacitor is connected to the integrator such that the output of the integrator ramps back to the voltage stored on the auto-zero capacitor. The number of counts required for the reference integrate phase is proportional to the input voltage. For this circuit, the reading displayed will

$$100 \times \left(\frac{Vin}{Vref} \right)$$

The final phase of the conversion cycle is the zero integrate phase. The purpose of this phase is to return the integrator output back to zero so that everything is ready for the next conversion cycle.

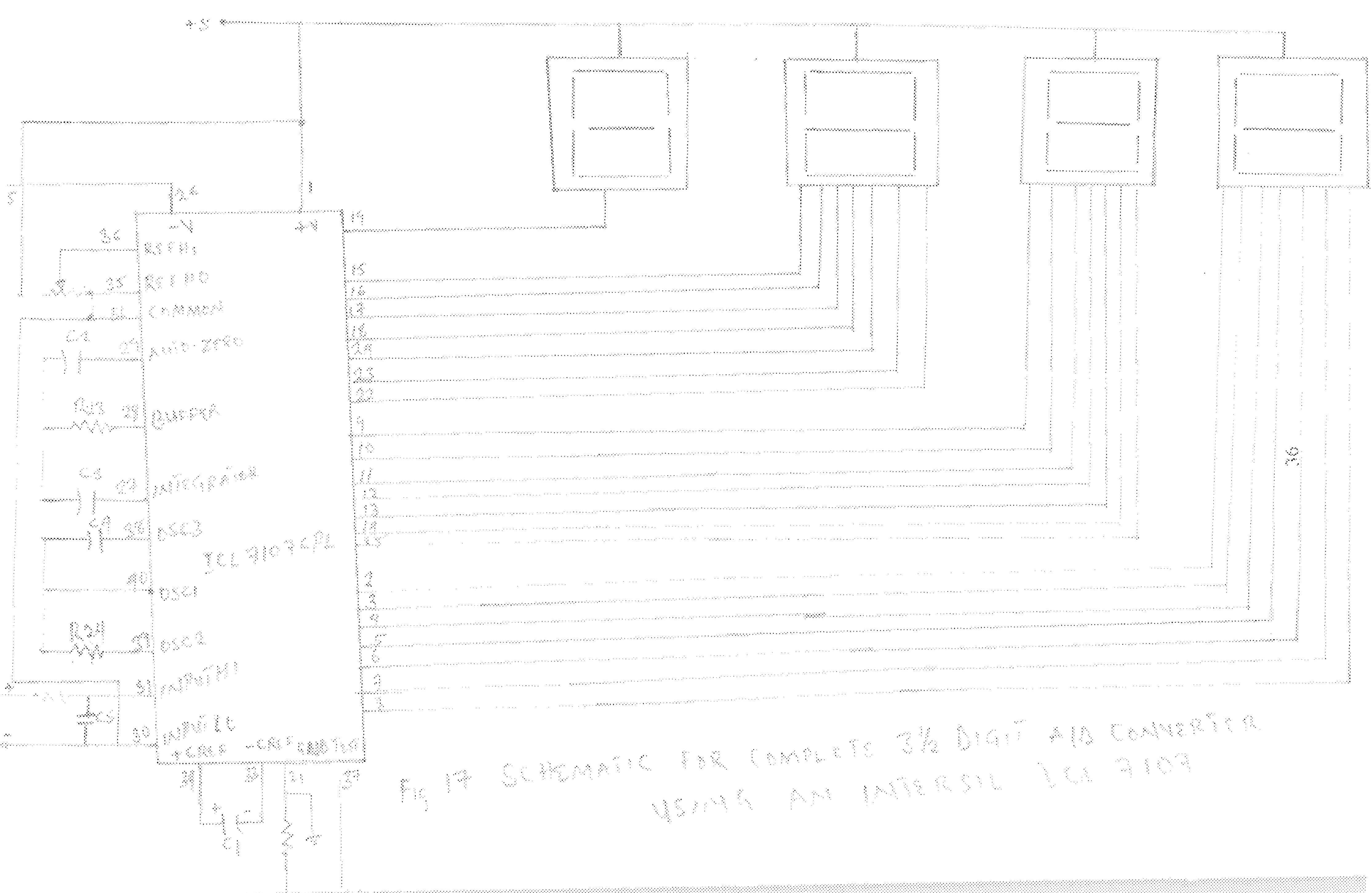


Fig 17 SCHEMATIC FOR COMPLETE 3½ DIGIT A/D CONVERTER USING AN INTERSL ICL 7107

2.4.4 Seven Segment Display

A very common output device used to display decimal number is the seven-segment LED displays packaged in various IC's formation seven segment display devices are used to convert a 4 bit BCD into a visible readout. It consist of seven LEDs arrayed as shown in fig 18 modern hand calculators, wristwatches, multimeters all uses the seven-segment-display for their readout. The LED type is cost efficient, reliable, comprisable and very bright and has a low voltage integrated circuitry.

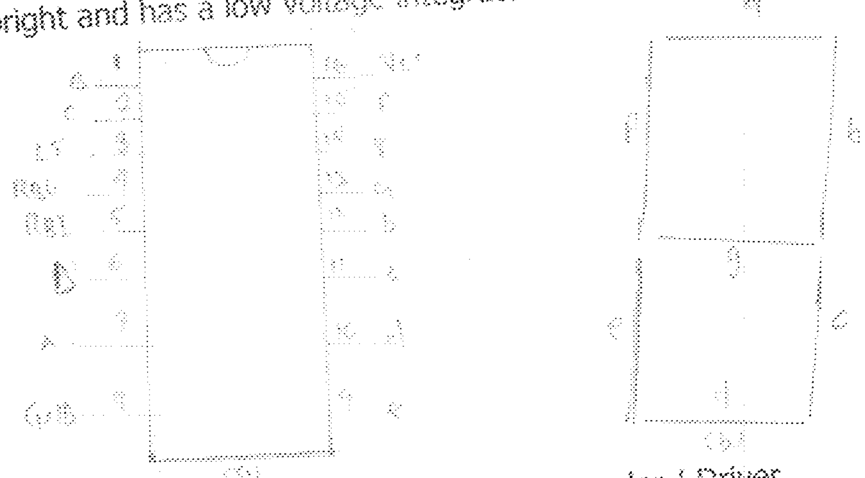


Figure 18 (a) Pin out for TTL 74LS47 Decoder / Driver
(b) Common –Anode seven- segment display

The segments of the seven-segment display turns on or light off that so closely approximate-the shape of the decimal digit equivalent to the binary value of the input for the common-anode display, all the anode LEDs are tied to V_{cc} while the cathode are connected to the decoder/driver through current limiting resistors of value 150ohms as shown in fig 18.1 below:-

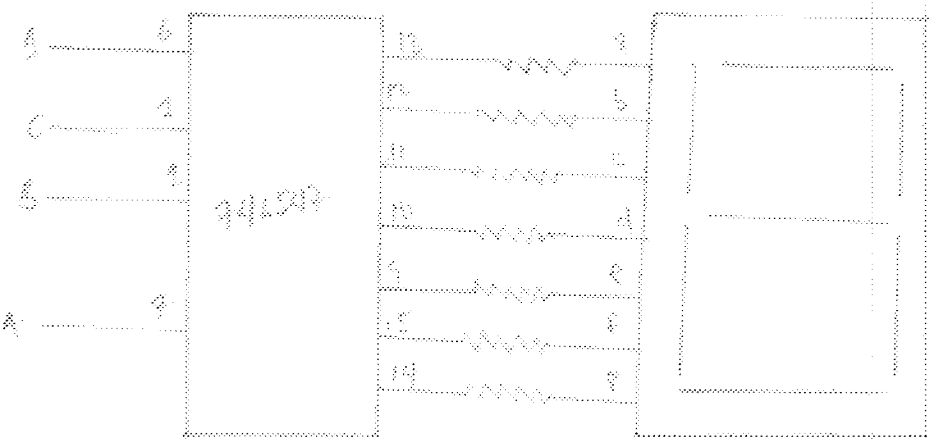


Fig 18.1 BCD – to – segment decoder/driver driving a common anode seven-segment LED display.

To illustrate the operation of this circuit let us suppose that LED inputs are D=0, C=1, B=0, A=1, which is 5 in decimal. With these inputs, the decoder/driver outputs $\overline{a}, \overline{f}, \overline{g}, \overline{c}$ and $\overline{d},$ will be driven LOW (connected to GND), allowing currents to flow through, $\overline{a}, \overline{f}, \overline{g}, \overline{c}$ and $\overline{d},$ LED segments and thereby displaying the numeral 5. The $\overline{b}$ and $\overline{e}$ outputs will be HIGH. So LEDs $\overline{b}$ and $\overline{e}$ will not conduct.

CHAPTER THREE

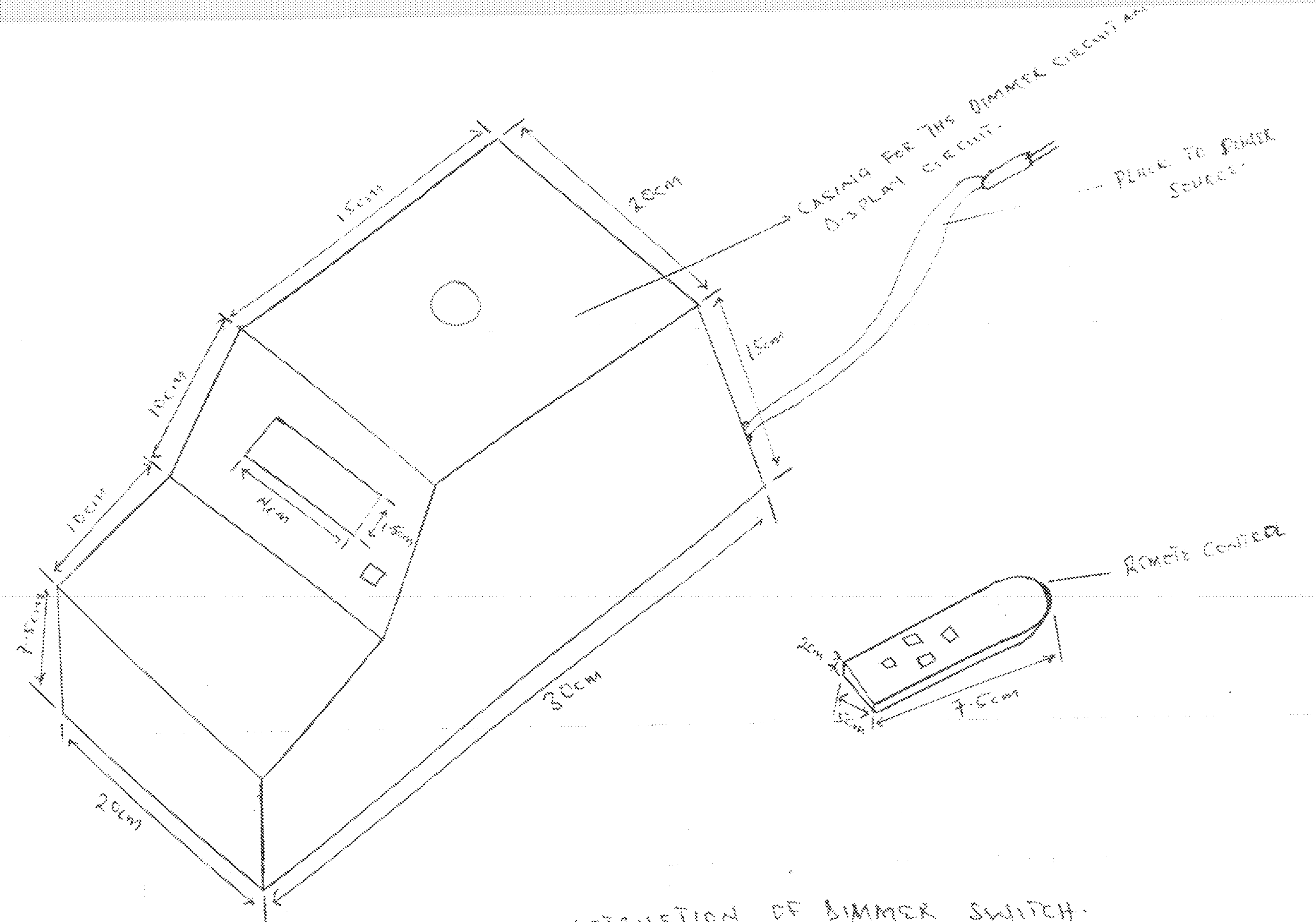
Construction and testing of result.

3.1 *Construction:*

The project was constructed based on the different building stages as indicated by the block diagram. The light dimmer was first built on bread board and tested, than transferred to veroboard, in the same way the display circuit was built as a separate unit before it was being in-corporated into the light dimmer circuit IC sockets were used to avoid damage to chips due to excessive heat during soldering.

The remote control receiver was built into the main dimmer circuit while the transmitter uses a separate potable casing and is battery operated. The transformer was crewed into the casing away from the main circuit to reduce effect of heat on discrete component and avoid the interference of flux developed from the transformer and flux developed by the inductor in the dimmer circuit.

The casing had a lamp-holder on which the test-bulb could be mounted and a socket outlet for connecting other loads. A window in front of the casing was also provided through which the infrared receiver could receive infrared signals.



CONSTRUCTION OF DIMMER SWITCH.

Figure 17

3.2 Testing of the Dimmer Circuit.

Different level of attenuation where selected at R=200kΩ the light came on and increased steadily to its full brightness at 0kΩ

Resistance (Ω)	Voltage (V)
0	220v
50	170v
100	120v
150	75v
200	40v
250	0v

3.3 Testing of Infrared Remote Control

At distance 200mm – 350mm the sensor controlled but above that it did not.

List of Components Used

S/no	Description of component	Quantity
1.	Resistors	36
2.	Potentiometers	2
3.	Diodes (IN4148 ZENER Diode)	3
4.	Diodes (1N4001, 400H)	1
5.	IC Regulators	2
6.	Bridge rectifier	1
7.	Choke resistor.	1
8.	NA 741	2
9.	Intersil 7107	1
10.	$3^1/_2$ digit segment display.	1
11.	Ceramic capacitors	9
12.	SC151E	1
13.	2N2926	2
14.	2N3702	1
15.	2N2646	1
16.	74ls93	1
17.	Cd4028	1
18.	CA3046	1
19.	BC109	3
20.	Tip 31	1
21.	BC 557	1
22.	BC 337	1
23.	IR diode	1
24.	IR sensor	1
25.	LED	2
26.	Electrolytic capacitor	4
27.	High voltage capacitor	1
28.	Transformer	1

CHAPTER FOUR.

4.1 *Conclusion*

From the table of result for the dimmer circuit it is observed that the voltage reduce as the resistance is been increased, that is to say that the aim of this project is achieved.

4.2 *Recommendations*

Regular power supply may not be guaranteed in Nigeria, therefore it is recommended that this project should be powered by a separate d.c power supply (e.g. 12V buttery).

If the project is to be developed for commercial purposes, provision must be made for it at the beginning of the construction of the building to ensure the cable connection are well concealed.

REFERENCES.

1. (http://www-s.ti.com/sc/psheets/sla5067/slaso67.pdf.)

2. Work out electronics by G. Water Worth.

3. Electronics: A course for Engineers by R.J. Maddock

4. Edward Hughes, (1995) Electrical Technology, 7th editions published by ELBs and longman group limited.

5. Mark N. Horentein, (1996), Micro Electronic circuit and devices, 2nd edition; published by Alan Apt.