DESIGN AND CONSTRUCTION OF HOURLY ALARM CLOCK SYSTEM

By

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99/9043EE

A project submitted to the Department of Electrical and Computer Engineering, School of Engineering and Engineering Technology,
Federal University of Technology, Minna.

In partial Fulfillment of the requirement for the award of Bachelor of Engineering (B.Eng) Degree in Electrical and Computer Engineering

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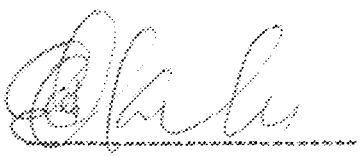
DECLARATION

I hereby declare that this project report, design and construction is the result of my work. It was conducted under the supervision of Engr. Abraham Usman of Electrical/Computer engineering department, Federal University of Technology Minna, Niger State.



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15/12/04
DATE

CERTIFICATION

This is to certify that this project titled "DESIGN AND CONSTRUCTION OF AN HOURLY ALARM CLOCK SYSTEM" was carried out by ERUNKULU OLAONIPEKUN .O under the supervision of Mr. Abraham Usman of Department of Electrical/Computer Engineering in the School of Engineering and Engineering Technology, Federal University of Technology, Minna.

..... 15/12/04.....

Mr. Abraham Usman — Date

(Project supervisor)

..... 15/12/2004.....

Engr. M.D Abdullahi — Date

(Head of Department)

....

External Examiner — Date

DEDICATION

I dedicate this project to the glory of God, my all in all, the ever faithful God. With Him the project had been a success.

I am also dedicating this project to my beloved parents, Mr. & Mrs. S.O. Erunkulu for their support. Also to my members of family; Mr & Mrs. A.O. Erunkulu, Miss Bola Erunkulu, Master Leke Erunkulu. Mr. & Mrs. Daramola.

My dedication also goes to my Course mates and my friends in general.

ACKNOWLEDGEMENT

I am most grateful to almighty God for the wisdom, knowledge and understanding he granted me during the cause of my project.

My profound gratitude goes to my supervisor Mr.. Abraham Usman for his assistance and guidance during this project. I also extend my thanks to my colleagues.

My appreciation goes to my parents Mr. & Mrs. S.O Erunkulu for their support both morally and financially and my sisters and brother

My sincere gratitude also goes to friends and loved ones, Pastor Rowland Okon, Tope Akinbosede, Sarah and Margaret Akpan, Shedrak, Yetunde Salami, Tope Ologun, Tunbosun Kolawole, Bukkola Salami and all my brethren for their love and support during the cause of my project.

ABSTRACT

The project describes the design and construction of a Digital hourly alarm clock System.

The clock is designed by the generation of a clock pulse from a crystal oscillator, divided and accumulated then to be displayed on the seven (7) segment display.

An alarm system is incorporated which sounds every hour, the number of time displayed. The alarm triggers when the pulse is sent to the alarm unit.

The whole system is powered from the 240V ac supply, but also has a backup battery incase of power outage, incorporated into the system. The clock is reset able to the desire time by the switches (control switches).

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CHAPTER ONE

INTRODUCTION

Time telling is an essential aspect of the life of human being. Man generally live by time because all his activity is based on time. The project is concentrated on the design and construction of a digital hourly alarm clock system.

The design circuitry consist mainly of three (3) basic sections namely, the clock unit (pulse generation unit), the alarm unit and the Power supply unit. The diagram in fig 1 shows the block diagram of an hourly alarm clock system.

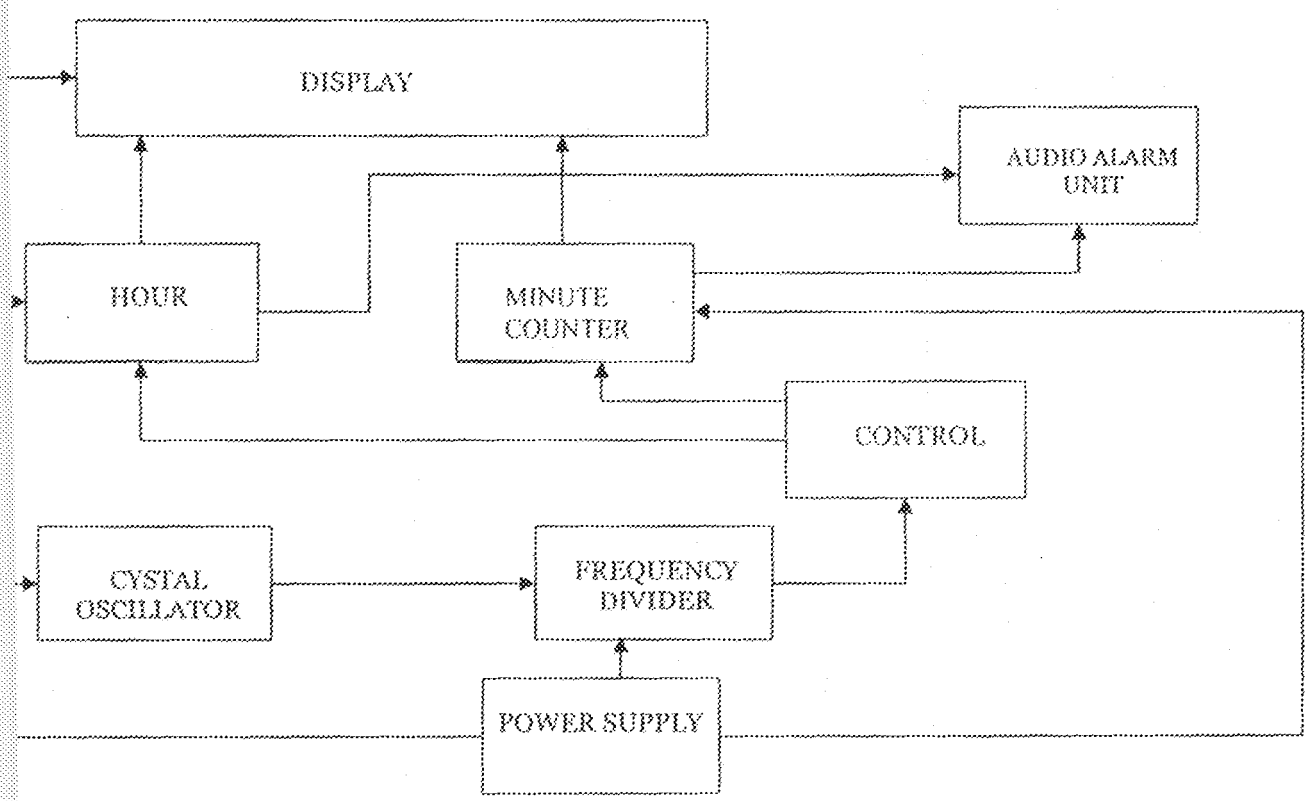


Fig 1. A BLOCK DIAGRAM OF HOURLY ALARM DIGITAL CLOCK

The clock unit is basically built on the generation of pulse which is achieved by the use of a crystal oscillator. This is further divided to give sixty (60) pulses per minute, that is , one second pulse per second (1pps) output. The decade counter sends the input signal to the 7 segment display which is decoded by the decoder. It also consists of control switches used in setting the desire time.

The alarm unit is designed to sound hourly, the number of times of the displayed time. This was achieved by a timer connected to two down counters. The time sends out the desire number of pulse to the speaker which produces the sound.

The power unit supplies the other main units with the desired voltage. The required voltage for this project is 5V D.C. the A.C main is converted to D.C and incorporated voltage regulator the 5V. Backup batteries were also incorporated into the circuit to keep the circuit on when the main supply fails. The batteries are rechargeable, when the main is on it charges, when off, the battery supply power to the system.

In construction of an accurate digital clock, a very closely controlled frequency is required. The frequency or pulse clock could be generated in different ways. In the case where AC power line is the source of pulse generation, a 50Hz or 60Hz power frequency is generated as the basic clock frequency before it is divided to one pulse per second (1pps). This however, is not stable as there are fluctuations in the pulse generated. In case of a DC operated clock, a 555 timer powered by the DC could be use to generate the pulse, this however is not also very stable. A more stable, accurate pulse

generation could be achieved by the use of a quartz crystal oscillator. This is used in this project for stable frequency generation.

1.2 LITERATURE REVIEW

Prehistoric man, by simple observation of the stars, changes in the season, day and night began to come up with very primitive method of measuring time. This was necessary for planning nomadic activity, farming, sacred feasts, and so on. The earliest time measurement devices before clocks and watches were the sundial, hourglass and water clock.

The forerunners to the sundial were poles and sticks as well as larger objects such as pyramids and other tall structures. Later the more formal sundial was invented. It is generally a round disk marked with the hours like a clock. It has an upright structure that casts a shadow on the disk - this is how time is measured with the sundial.

The hourglass was also used in ancient times. It was made up of two rounded glass bulbs connected by a narrow neck of glass between them. When the hourglass is turned upside down, a measured amount of sand particles stream through from the top to bottom bulb of glass. Today's egg timers are modern versions of the hourglass.

Another ancient time measurer was the water clock or clepsydra. It was an evenly marked container with a spout in which water dripped out. As the water dripped out of the container one could note by the water level against the markings what time it was.

One of the earliest clocks was invented by Pope Sylvester II in the 990s. A huge advance occurred in the 1300's when mechanical clocks, which used weights or springs, began to appear. At first, they had no faces, and no hour or minute hands; rather, they struck a bell every hour. Later, clocks with hour, and then minute hands began to appear. These early mechanical clocks worked by using an escapement, a lever that pivoted and meshed with a toothed wheel at certain intervals.

In the 1400's, another important discovery in timekeeping was made: it was learned that coiled springs, which used small coiled springs unwinding at a speed controlled by an escapement, were able to move the hands on a clock as well as weights or springs of previous, larger clocks. This discovery made smaller clocks, and later watches.

In 1656, Christiaan Huygens invented the pendulum clock, which used weights and a swinging pendulum. These clocks were much more accurate than previous clocks, off by less than a minute a day, compared to the 15 minutes a day of earlier clocks. The bigger the pendulum, the more accurate the clock was. In 1761, John Harrison succeeded at inventing a small clock accurate enough to use for navigation at sea.

Electric clocks came into being after 1850, when Eli Terry developed machines, patterns, and techniques that produced clock parts that were exactly alike. An electric motor with alternating current powers these clocks. Later digital clocks with LCD (liquid crystal displays) rivaled the electric clocks. Quartz clocks use the vibrations of a quartz crystal to power the clock.

There two basic types of clock used today; digital timepieces which is a digital display of the time in numbers. While the Standard uses the three arms pointing to the number to indicate hour and minute.

Both of the basic type could have alarm system which sounds, at a set time or hourly indicator as the case might be. Some make melodious sound, some a beep sound while, improved one will speak the time.

This project is widely useful to both the students and the entire staff of the school. It updates them of the current time by sounding hourly. This enables both the students and lecturers to be aware of their next lecture period and when it is through. The library for instant is updated with the time, when to open and close to the students. Also it can be use in manufacturing industries, where they do shifting. In the hospital, this keep both the patients and staff about time to take medical record, treat a patient, or do regularly check up. It is applicable to all fields.

CHAPTER TWO

PROJECT DESIGN

INTRODUCTION

There are three (3) main stages of the whole circuit namely; the POWER SUPPLY, the CLOCK SECTION, and the ALARM SECTION. These are further subdivided, for instance, the power supply has both the main (ac) source and a backup (dc) unit. The Clock section has the pulse generator, frequency divider, control, count accumulator, decoder and the display. The Alarm unit has decade counters, timer and an output media (speaker).

2.1 THE POWER SUPPLY

2.1.1 THE MAIN (AC) SUPPLY

The circuit requires a 5V dc supply to drive it. The mains is a 240V ac supply, this however, is needed to be rectified to give a dc output. By mean of a rectifier connected to the source will convert the ac input to dc output, this however consists of both the ac and dc components. The ac component is needed to be filtered out for a proper operation of digital clock, and this was achieved by a capacitor connected across the output. The filtered output which is 12V was regulated by LM 7805 IC to the desired voltage of 5V. Fig 2.0 shows the basic representation of voltage conversion

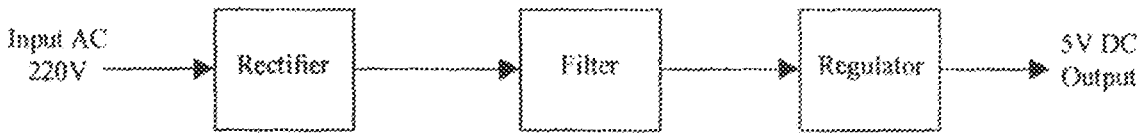


Fig 2.0 BLOCKS DIAGRAM OF VOLTAGE CONVERSION

RECTIFICATION

The rectifying circuit converts the input ac source to a dc supply, needed by the circuit to drive it. There are different rectifications circuits that can convert ac to dc, among this are the Half wave rectifier, Full wave rectifier. For this project the Bridge rectification was employed to convert the ac to dc, in order to have a steady dc input.

The Bridge rectifier consists of four (4) diodes, D_1, D_2, D_3, D_4. The input voltage is sinusoidal, that is the voltage has both the positive voltage, V_w Cos wt, and the negative voltage - V_w Cos wt. During the positive voltage input, diodes D_1 and D_4 are forward biased, therefore conducts, this form the wave form. On the negative voltage input, the two other diodes D_2, D_3, conducts to form another half cycle. Hereby, eliminating the negative half cycle. Both current pass through in the same direction to give a fluctuating unidirectional voltage. The waveform is shown in the fig 2.1 below.

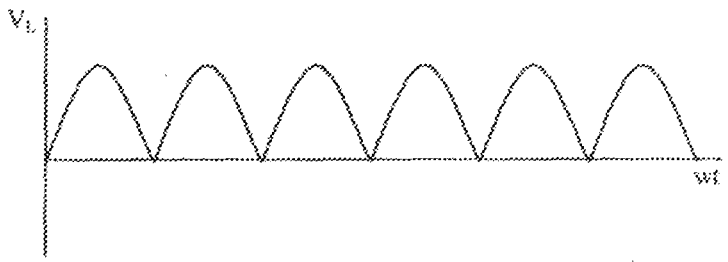


Fig 2.1 WAVEFORM OF A FILTERED RECTIFIER

The ac ripple in the output of the rectifier can be smoothed by a filter circuit. This is achieved by a capacitor connected across the output of the rectifier. Another capacitor is connected which is a high frequency filter, it surpasses the high frequency power due to oscillator divider. Then tapping of the load across the capacitor to the regulator input, which regulated the input voltage from 12V to 5V.

2.1.2 BACKUP POWER SUPPLY

Two 6V rechargeable batteries were connected to the circuit to keep driving the circuit incases of power outage. The batteries are recharged when the main is on. On power outage, the batteries back up the circuit by supplying the required voltage to drive the circuit.

A Diode is installed at the output of the rectifier to prevent backward flow of current, in case of power outage by the mains. The output of the batteries 12V is regulated to supply 5V desired to power the circuit. Fig 2.3 shows the power supply

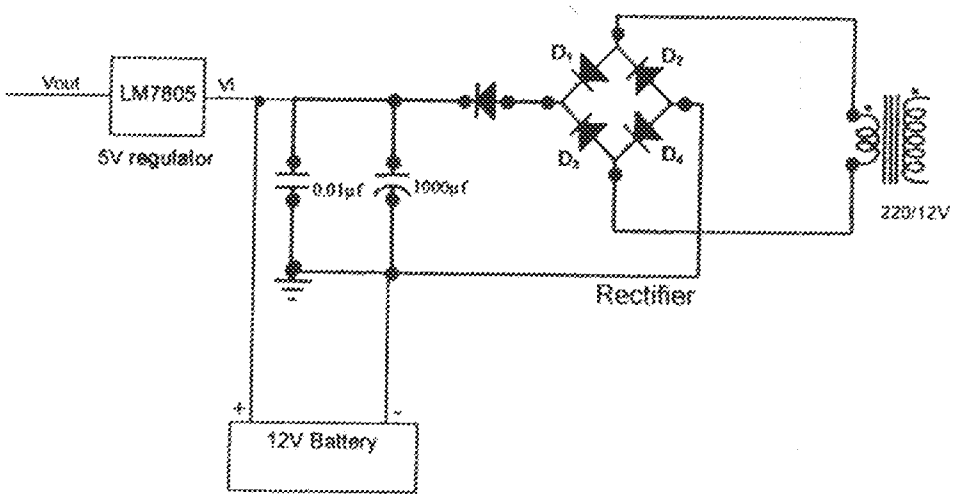


Fig 2.3 POWER SUPPLY UNIT

2.2 THE CLOCK SECTION

This section described the design of the clock which consists of different subsections, the pulse generator (Timer), the frequency divider, count accumulator, decoder and the display unit.

2.2.1 PULSE GENERATION (TIMER)

The timer is responsible for the generation of timed pulses counted by the counter. This was achieved by the use of a quartz crystal oscillator in this project. These generated pulses are accurate and stable. There are other astable multivibrators, such as 555 Timer, but this is not as stable in pulse generation as that of the quartz crystal oscillator used in this project.

QUARTZ CRYSTAL OSCILLATOR

It main function is to control the oscillation of an electric current, the frequency of which is reduced to compute time. They are made from CMOS, Complimentary Metal Oxide Semi conductor. It consists of two MOS FET integrated on a silicon chip. They are easily damage by static electricity.

The error by quartz crystal is plus or minus one second in ten years. The accuracy of the quartz crystal clock is very high and reliable. The extremely high quality factor or quartz crystal applied to oscillator led to very stable frequency value such as ones used in timing circuit and clock signal generation. Below fig 2.3 show the crystal oscillator

Fig 2.3 QUARTZ CRYSTAL OSCILLATOR

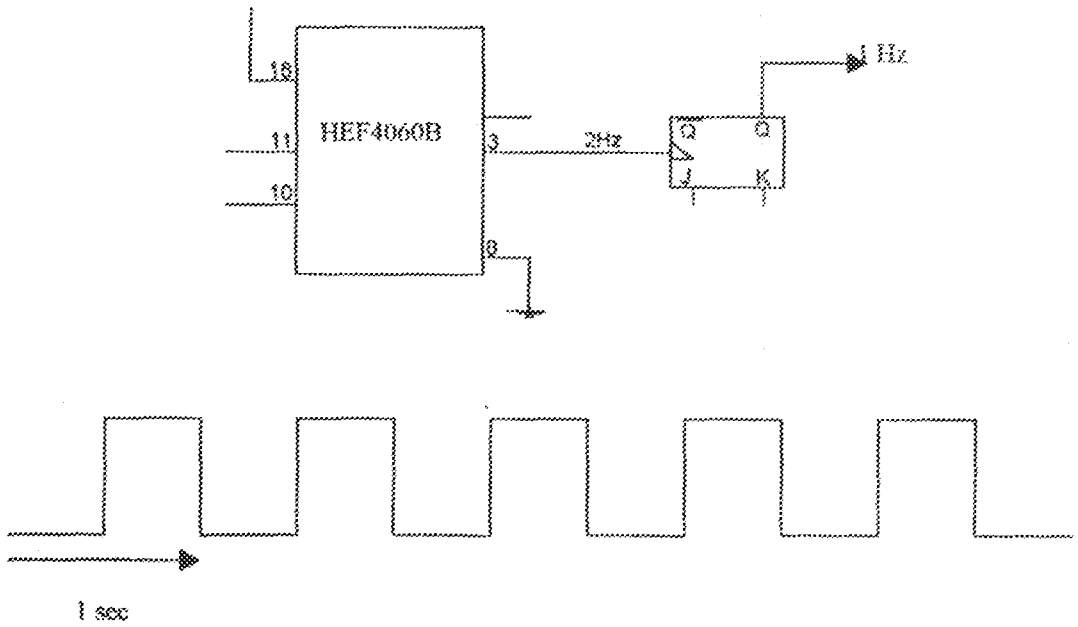
2.2.2 THE FREQUENCY DIVIDER

The generation of the clock pulse or frequency of 32.768Hz from the quartz crystal oscillator needed to be divided to give one (1)Hz output needed by the circuit. The application of a HCF 4060B IC which can be used as an oscillator divider along with a toggle (JK) flip-flop was employed to get the desired 1Hz.

The HCF4060B IC consists of an oscillator section and 14 ripple carry binary counter/divider stages or flip-flop stages responsible for the division of the input signal from the crystal oscillator of 32.768KHz by a factor of fourteen (14) to give an output of 2Hz, at the pin 3.

$$\text{Output frequency} = \frac{32.768K}{2^{14}}$$

$$= 2Hz$$



The required frequency is 1Hz, but the output of the HCF4060 IC is 2Hz. therefore, there is need for further division. This can be easily achieved by the use of an external toggle (JK) flip-flop. Connecting of a HEF4027B dual JK flip-flop made this possible.

The JK flip-flop is one of the memory elements used for counters. When J = 1 and K = 1, the circuit toggles and compliment the output. The transition table shows the time sequence of inputs, outputs and the state of the flip-flop. x represents the Don't Care condition.

Present output	Next state output	Required inputs	
Q	Q (t=1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

TRANSITION TABLE OF JK FLIP-FLOP

2.2.3 THE COUNT ACCUMULATOR

This consists of counters (HEF4520B IC) that keep track of the number of seconds from 00 through 59 and then reset it to 00 with an output of one pulse per minute.

The HEF4520B IC is a dual 4-bit internally synchronous binary counter, each can count from 0 – 15, by cascading both together, It gives a 8-bit counter which could count for 0 – 256, 2^8. It is designed to count sixty pulses then it sends out a pulse. The AND gates detect 60 (00111100) pulses. The IC being a dual binary counter, the first counts to 0011, on getting to this count, the AND gate detect it and send a high to the input of the other AND gate. While the other counts to 1100, the diode detect it and both high input to the AND gate to give an output of 1, which is the 60 second pulse. There is a feed back to the ICs to avoid having a count greater than 60.

2.2.4 MINUTE COUNTERS

For every sixty counts (seconds), a signal is sent out to the decade counter which triggers it. This was achieved by the use of two HEF4029B ICs. The HEF4029B is synchronous up/down 4-bit binary/BCD decade counter. Here, the counter was used as an up counter.

Each of the counter can count from 0 – 9, cascading the two counters by joining pin 7 and 5 respectively give a configuration that can count from 00 – 99. For every 60 second pulse, there is a signal sent to the decade counter

which count as one. It increment for every minute. When the first counter gets to 9, at the incoming of the next impulse, it is reset to zero, then it send the signal to the second counter which reads as 1.

When it reaches 60 minutes that is it had counted to 59, then to 60 at the next in coming of the pulse. The AND gate detects the 60, instead of displaying the 60, the OR and AND gate clear off the other figures and reset it to zero. Then a pulse is sent out to the hour hand counter. Pin 4, 12, 13 and 3 serve as the preset able inputs. When pin 1 is active high, it jams the input code to the output as the code to be displayed.

2.2.5 HOUR COUNTERS

This also consists of two decade (HEF4029B) Counter, also used as an up counter. It is designed to count from 01 – 12, as the hour. The last counter can only count from 0 -1.

The output pulse from the minute counter triggers the hour counter, it receives it as a pulse to be display as 1. for every 60 minute pulse, a pulse is sent out and there is an increment in the hour counter. The first counter counts from 0 – 9, when it get to 9 any incoming pulse reset it to zero and it sends a pulse to the other counter.

For the hour of the clock, we can only have a display of 12 hours. Therefore, when the counter counts to 12, an incoming pulse which is meant to make it 13, is cut off and reset to 00. This was possible by the two AND gates connected which sends a pulse to the preset pin 1. Whenever there is a

binary code combination of 0001(1) and 0011 (3), the AND gate detect and send a pulse to reset it to 00.

2.2.6 DISPLAY UNIT

BUFFER (MULTIPLEXERS)

The CD4503B is a hex non inverting buffer with 3-state output having high sink and source-current capability. The output is the same as the input, it has enabling input, which is used to enable or cut off the output of the input. It joins two or more buffer together, it is active LOW, that is, 0 (LOW) enables the output of the input while when high, disable the output.

It has six (6) buffers, but for this project I am making use of four (4), it has a common enabling input. The mechanism of the buffer is used to multiplex the outputs of the counters towards the only decoder (HEF4511B), which display the output on the 7-segment display. Fig 2.5 shows the functional diagram of buffer

Conventional frequency for multiplexing is 1 KHz, this was achieved from pin 5 of the 4060B IC. Period between each of the pulses is $T = 1/f_m$. This made it impossible to human eyes the transition

Where $C = \frac{32.768K}{2^5} = 1.024KHz$

Period $T = 1/f_m = 0.0009765625s$

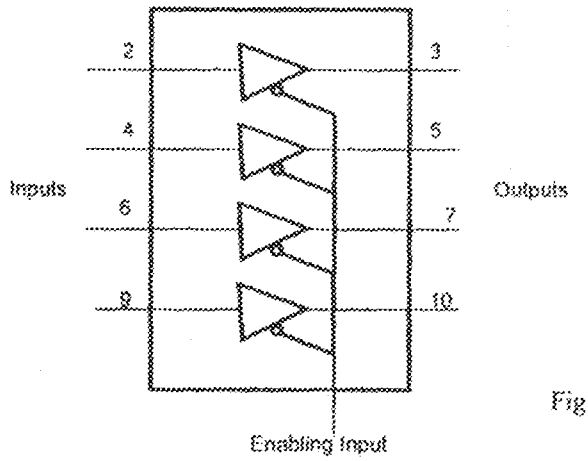


Fig 2.5 CD4503B BUFFER

2.2.7 STEPPER

The HEF4017B is an example of a Decade counter, decade counters enable a clock pulse to be counted or divided, and it is a five (5) stage. The HEF4017B has 10 output pins, when pin 14 is connected to an astable 'clock' input and pins 16 and 8 are connected to a suitable power supply.

This serves as the HEART (Control) of the multiplexing. Only one output of HEF4017B is high for ever clock input. It has ten (10) outputs, but for this project, I'm making use of four (4) outputs. To cut off the other six outputs, the 5th output pin 10 is feedback to the reset pin 15, this send it back to the starting pin 3, hereby using only four (4) active outputs.

The clock input at pin 14 comes from pin 7 of the 4060B, for every clock input, it increments hereby, causing it to move from one buffer to the other to select it.

CLOCK	1	2	3	4
A	1	0	0	0
B	0	1	0	0
C	0	0	1	0
D	0	0	0	1

The output clock which is high only once will select the buffer 4503B on after the other. When the output of pin 3 (A) is HIGH, all others are LOW, therefore, the first buffer is selected to send its output binary code to decode. The same goes for the others as shown in the true table above.

The buffer is active LOW, but the signal sent to it is high, therefore the need of an inverter comes in. an inverter is connected to the input pin 1 of the buffer, which invert the incoming high signal to a low pulse to enable the buffer. The active low is shown in the true table below

CLOCK	1	2	3	4
A	0	1	1	1
B	1	0	1	1
C	1	1	0	1
D	1	1	1	0

2.2.8 DECODER/DRIVER

In digital electronics, all operations are carried out in binary form. The output information at the counter are in binary form, therefore, need arise for converting the form suitable for a man to interpret. This required the use of a "DECODER".

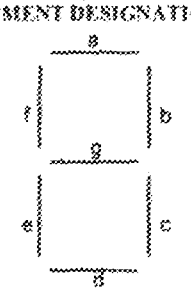
A Decoder is a combinational logic circuit that converts binary codes from n-input lines to a maximum of 2^n unique output lines.

For this project, a HEF4511B decoder was used. The decoder is a BCD to 7-segment decoder/driver with four inputs, with seven high active outputs. It is a common cathode. The selected buffer sends the information which triggers the decoder. It decodes the incoming binary codes at the pin 1, 2, 6, 7 then, jams it to the display segment through the output pins 9, 10, 11, 12, 13, 14, and 15. Below shows the true table of HEF4511B decoder.

INPUTS				OUTPUTS							
D	C	B	A	O_a	O_b	O_c	O_d	O_e	O_f	O_g	Display
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	0	0	1	1	9

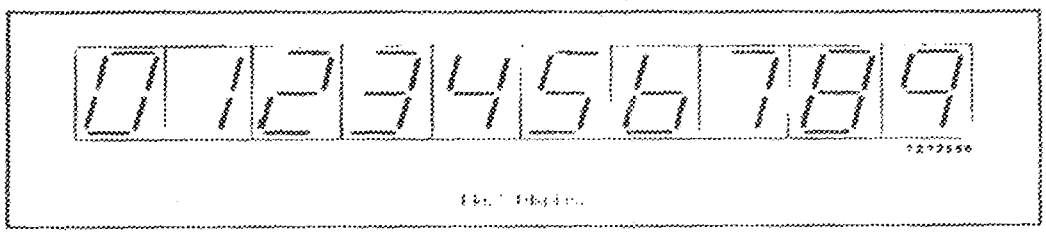
FUNCTION TABLE OF HEF4511B DECODER

SEGMENT DESIGNATION



BCD to 7-segment latch/decoder/driver

HEF4511B
MSI



2.2.9 DISPLAY

Four 7-segments displays were used in this project to display the time output. The display itself is made up of 7 LED (light-emitting diode) segments linked together via a common anode connection. Each of the four displays is connected in parallel. The decoder used here is a common cathode connection, while the display is a common anode. Therefore, for capabilities, an inverter was connected to each of the output lines of the decoder. Each diode has its own current-limiting resistor of 220 ohms.

The displays are also multiplexed, because of the connection, if not multiplexed, the information sent by the decoder will be displayed at all the 7-segment display. This was achieved by the use of PNP transistors drivers. They are inverted to turn them to common cathode, each having a limiting current resistor of 220 ohms. The output of the stepper, which is active high, is inverted to active low, select which display is to be enabled. The other ones are disabled.

2.3 ALARM SECTION

This section is responsible for the output sound. It consist of two counters (HEF4029B), timer (HEF4017B), SR flip-flop (HEF4027B) and the output speaker.

The HEF4029 is a synchronous up/down 4-bit binary/BCD decade counter, it could be used as a up or down counter. For this section, they are being used as down counters. The two counters were cascaded by joining pin 5 and

pin 7 together. The configuration of the two gave a 8-bit binary down counter.

They serve as the input Hour time into the alarm unit. The outputs of the hour counter are connected to the input of the counter as shown in fig 2.6

The OR gate connected to the output pins of the minute counter is a zero detector, it detect when the output is zero then sends a low signal which is inverted to the AND gate. The other input from the 60 second pulse is also high. Both inputs gave a high output at the AND gate, this preset the two counters by jamming the input data to the outputs.

At the same time the set pin of the SR flip-flop became high. The Q output becomes high while, $\bar{Q}$ became low. For the sound to be heard, an audio frequency is needed. This was achieved from pin6 of the 4060B, the output frequency; 256Hz, was connected both with the Q signal fro the flip-flop to the input of the AND gate to give the output of the audio frequency.

At the timer (4017B), when pin 15 (reset) is high, the timer is disabled, therefore becomes enable at active low. The output of the flip-flop complement, activate the timer. The timer need clock pulse, this was achieved from pin 2 of 4060B to the pin 14 of the timer. For every clock, it gives an active high output at pin 2, this is connected along with the audio frequency as the input of the AND gate which sends out a pulse which triggers the speaker and a sound is heard.

The output signal form the timer also clock the down counter at the same time, this causes it to decrement. That is, counting downward the input time. When it get to zero, the pin7 of both IC becomes zero, the zero detector detect it, the output was inverted which made it high to reset the flip-flop. The AND and OR gates allow the sound before it reset when it get to zero.

CHAPTER THREE

CONSTRUCTION AND TESTING

3.1 CONSTRUCTION

The design specifications are greatly considered when constructing each section of the digital clock with hourly alarm system. The need to classify logic families is essential; there are earlier types such as Register Logic, Resistor Transistor Logic (RTL) and Transistor Logic (DTL) these had been superceded by the Transistor – Transistor Logic (TTL). This was used for the project. In order to avoid problems associated with interfacing different logics.

The constructions of each section are elaborated below.

A transformer rating 220V, 500mA (primary and 12V on the secondary, feeds the bridge rectifier, which was constructed with 4 diodes (IN4001). The output voltage was filtered by a capacitor rating 1000μf, a regulator was connected to regulate it to 5V required by the circuit. Two rechargeable batteries were connected to the output of the filtered 12V, the purpose is to backup the system incase of power failure. The filtered voltage also charges it.

The pulse generator was constructed using a quartz crystal oscillator, there are other astable multi-vibrators such as 555 timer, but it is not as stable as

the crystal oscillator. The output frequency of the quartz crystal oscillator gave 32.768 KHz.

A divider with 14 stages and flip-flop were connected in series gave an output of one pulse per second (1pps), this serves as the required pulse generation. Count accumulator was constructed with the use of dual binary counters.

The minute counters were constructed with the use of two decade up counters, pins 4, 12, 13, 3 were grounded, pins 6, 11, 14, 2 serve as the outputs to the decoder. Pin 15 is the clock input. For the hour counters, two decade counters were used for the construction, all input pins were grounded except pin 3 of the first hour counter to reset to 00 when the time get to 13hr.

In the construction of the display, multiplexing principle was employed. Four buffers, 1 decoder, a stepper and 4 7-segment display were used for the construction. The stepper controls the choice of the buffer and that of the 7-sement display. The limiting resistors of 220Ω were used to reduce the output of the decoder current to the 7-segment display.

The alarm unit was constructed with the use of down counters/zero detectors, timer, SR flip-flop, and the speaker. The flip-flop serves as the control of the unit, it activates the timer for the incoming signal, then deactivate it. It controls the signal sending of the counters likewise.

The whole sections were interlinked, such that the output of one stage serves as the input of another stage.

3.2 TESTING

Components used were tested before usage in the project. The rating of the capacitors, resistors were ensured.

On powering the circuit, the output of each of the pulse generators, counters and logic sequential circuit were tested by LED. Each of the stages was tested to ensure required output. The soldering techniques were employed to ensure no damage to the ICs.

At the end of all connection and testing, the system was counting and displaying of Hours, Minutes and sound at every hour. This justified the design and construction.

CHAPTER FOUR

CONCLUSION AND RECOMMENDATION

4.1 RECOMMENDATION

In case of power outage, the backup batteries can power the circuit but the time might not be long, therefore a much bigger capacity of batteries is recommended. There is also no indicator of the second section. This could be replaced by a 7-segment display.

The alarm sounds the displayed time. A better project could be achieved, if the time is said rather than beep sounds

I also recommend a microprocessor chip to be used in future, this will reduce the complexity and bulkiness of the circuit.

4.2 CONCLUSION

It could be deduced after testing each stage, that digital clock with an hourly alarm system can be designed and constructed from the basic principle of electronics counting.

With the use of counters, I come to a conclusion that counters can be used not only for counting figure but much more, such as for digital clock among

others. The project shows that the theoretical values tally with the practical values.

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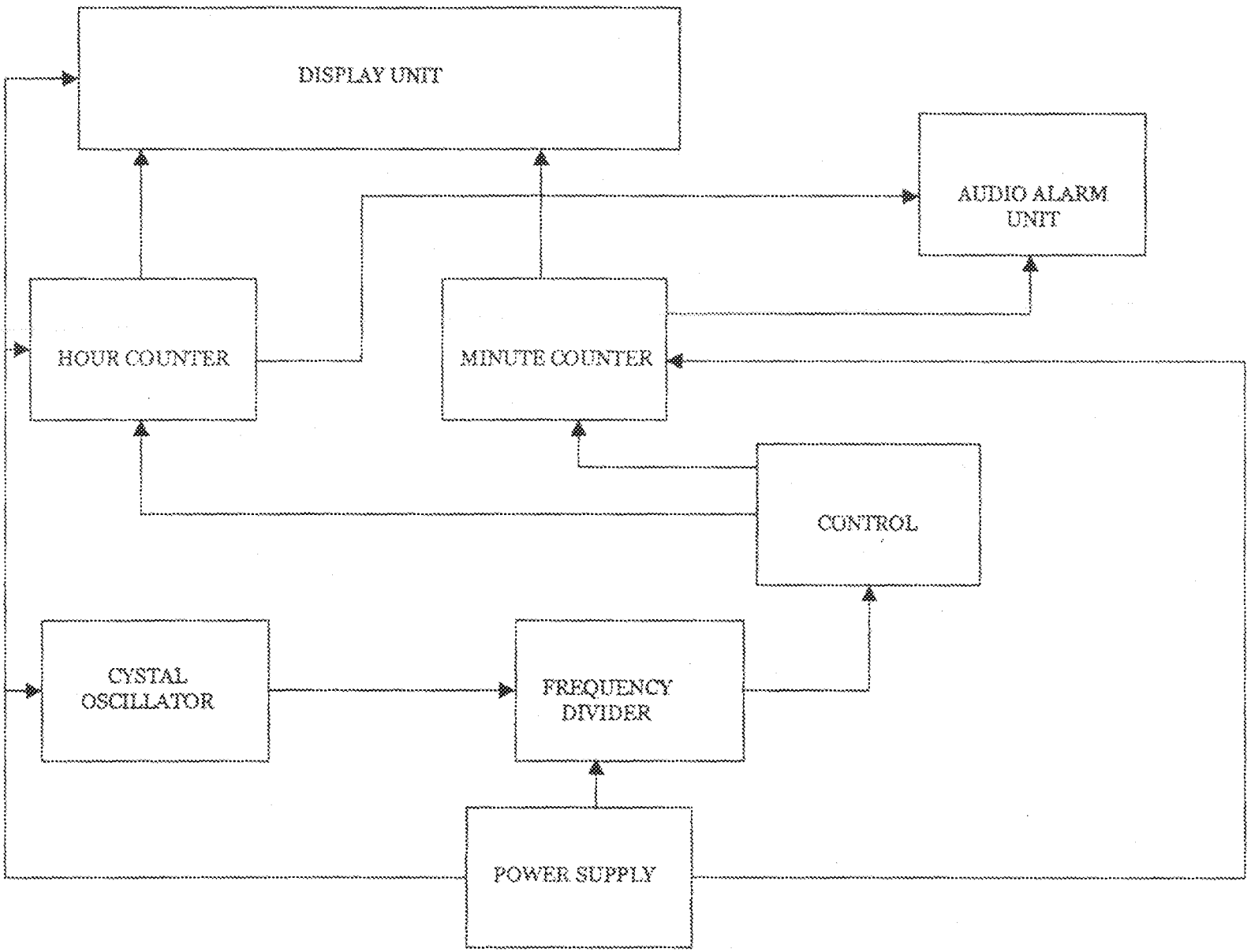

Fig 1 A BLOCK DIAGRAM OF HOURLY ALARM DIGITAL CLOCK

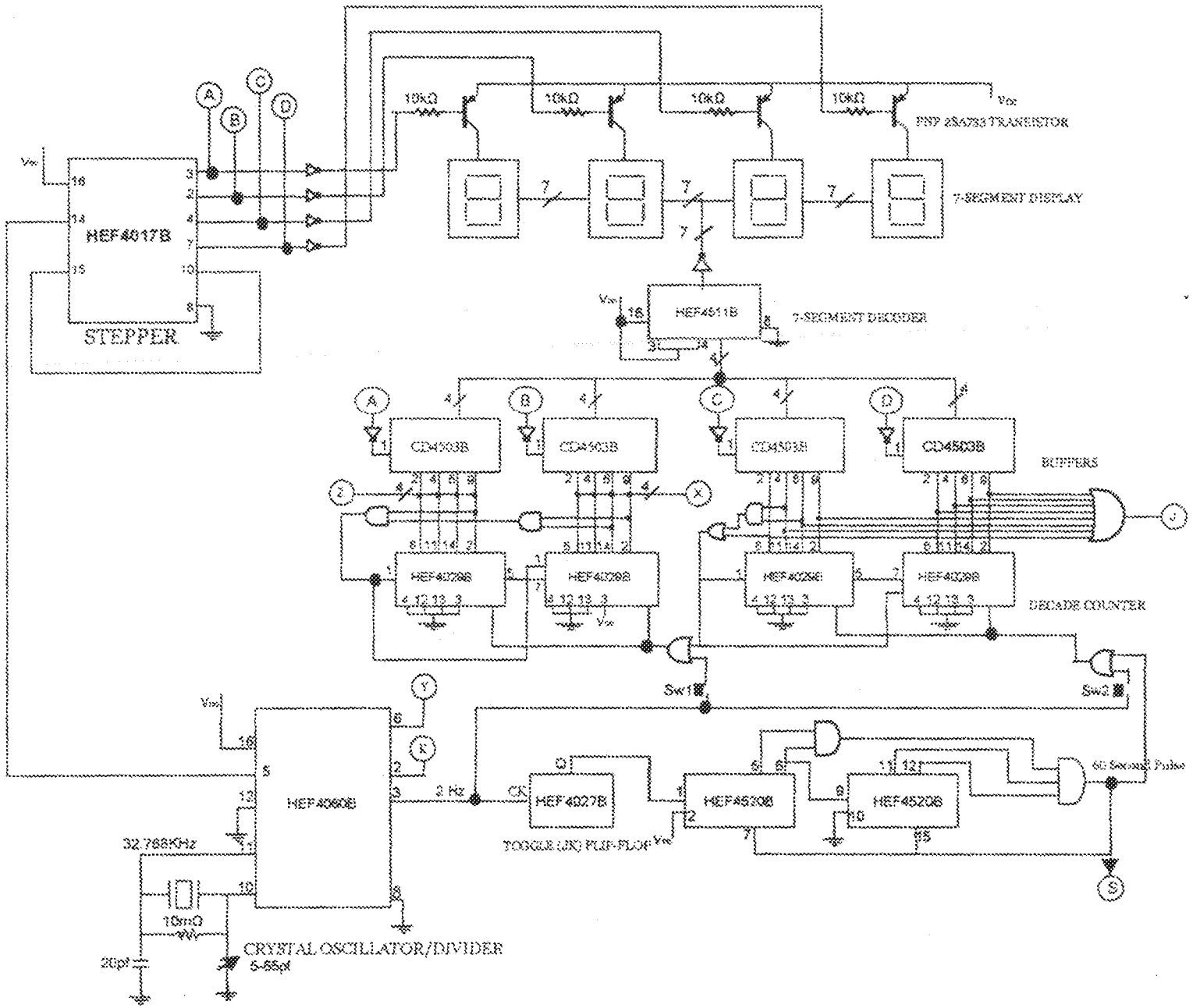

FIG 2.5 CIRCUIT DIAGRAM OF THE CLOCK UNIT

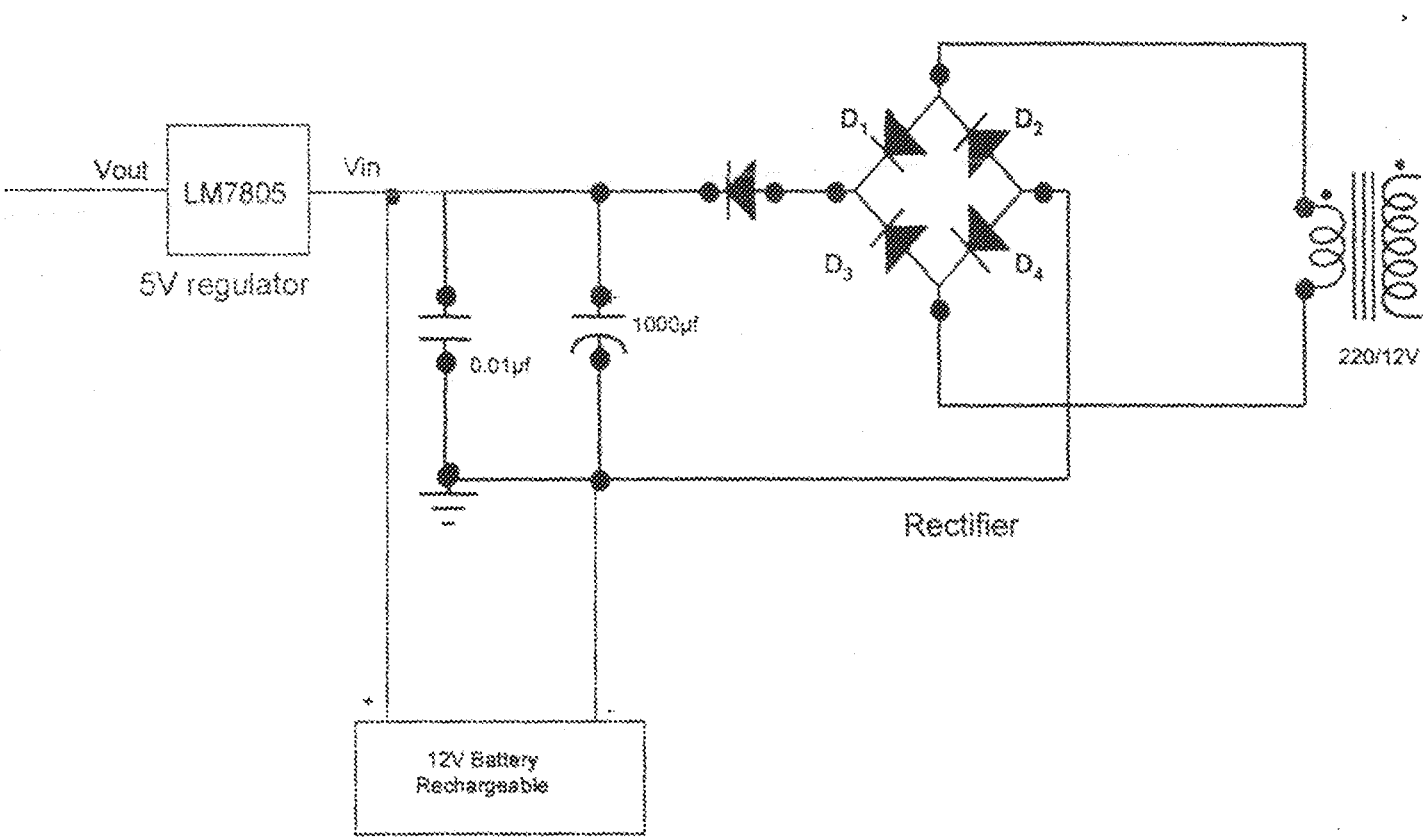

Fig 2.3 POWER SUPPLY UNIT

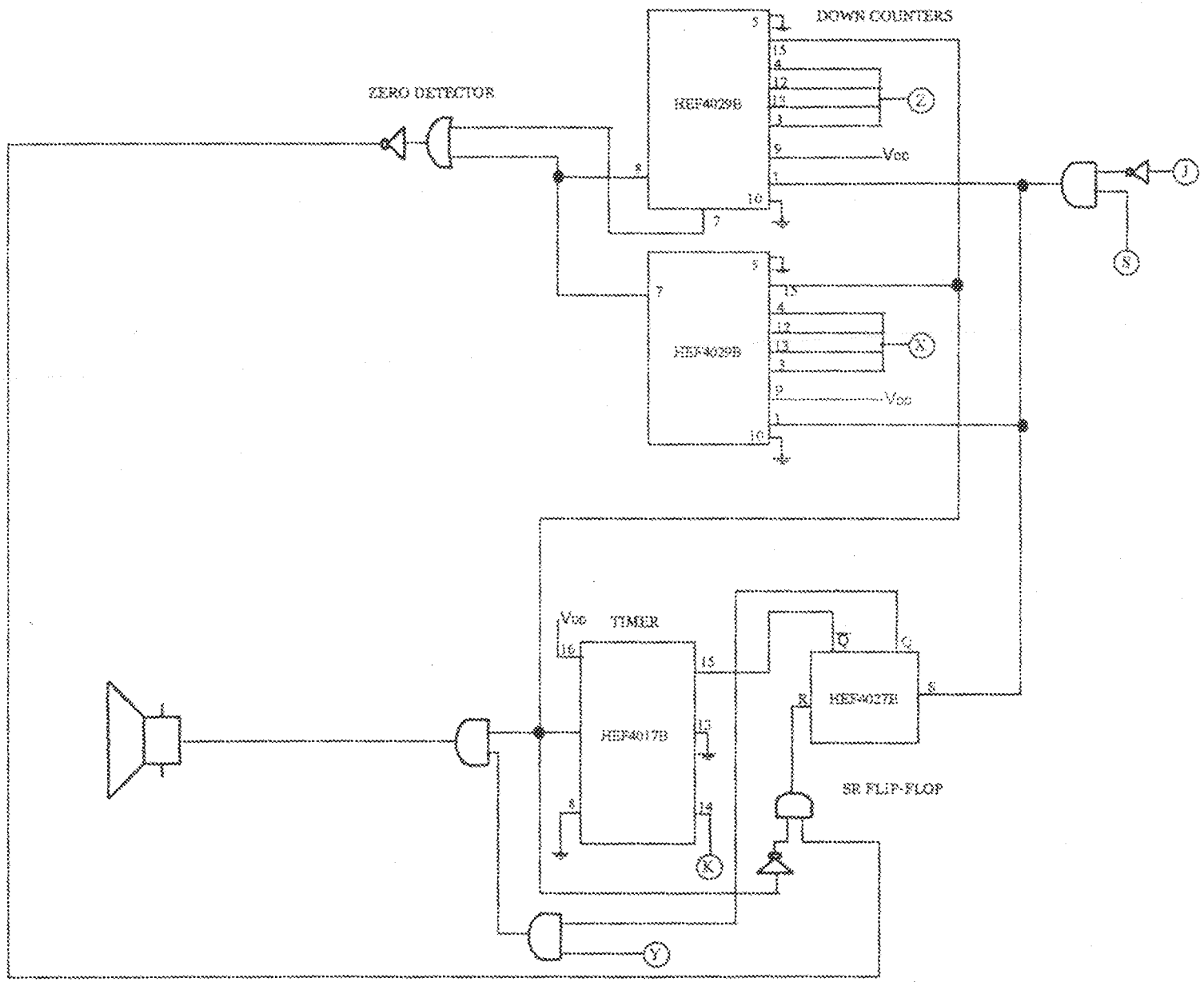

FIG 2.6 A CIRCUIT DIAGRAM OF THE ALARM UNIT