DESIGN AND CONSTRUCTION OF RADIO FREQUENCY DETECTOR (RFD)

BY

GARBA MUSA

(95/4549EE)

A Project Report Submitted In Partial Fulfilment Of The Requirements For The Award Of Bachelor Of Engineering (B.ENG.)

Degree in the

Department of electrical and Computer Engineering,

School Of Engineering and Engineering Technology,

Federal University Of Technology, Minna, Nigeria.

December, 2000.

CERTIFICATION

This piece of work on the design and construction of Radio Frequency detector (RFD) has been approved as partial fulfilment of requirement, for the award of B. Engineering in Electrical and Computer Engineering in the School of Engineering and Engineering Technology, Federal University of Technology, Minna, Niger State.

Supervisor sign — Date

(MR. PAUL ATTAH)

H.O.D. sign — Date

(ENGR. DR. Y. A. ADEDIRAN)

External Examiner sign — Date 17/1/2023

DECLARATION

I hereby declare that this project is an original work of Garba Musa (95/4549) and to the best of my knowledge has never been presented elsewhere for the award of degree or diploma.

However, this project work is based on the information obtained from record texts and observations all of which are acknowledged.

....

GARBA MUSA & SIGN DATE

ACKNOWLEDGEMENT

All glory must be given to the MOST HIGH GOD for his mercies, love and kindness bestowed on me before and during the course of my degree program and for the successful completion of all my endeavours at the Federal University of Technology, Minna.

My profound appreciation goes to my dearest Mum: Mrs. Comfort Oseh for all her untiring efforts towards my physical and academic upbringing, to my father Mr. Felix Oseh, for his support and to my step Mum as well.

Inclusively, my outstanding brothers and sisters are recognisably appreciated: Engr. Kayode Oseh, Mr. Abiodun Ogar, Mr. Olu Ogar, Miss Catherine Oseh, Mr. Sunday Oseh, Idowu Oseh, Engr. Emmanuel Oseh, Mr. Michael Oseh, Friday Oseh, Alaba Oseh and Kemi Oseh for their moral and substantial assistance.

Importantly, I thank the Head of Department of Electrical/Computer Engineering: Engr. (Dr.) Y. A. Adediran who made positive contributions to my project and my able supervisor: Mr. Paul Attah who was a tolerable and patient supervisor, a reliable counsellor and an understanding friend.

History will not forgive me if I fail to express my earnest appreciation to my pastor, brother and friend: Pastor Patrick ChurchHill of Love Chapel, Kontagora to whom I owe a great deal of gratitude.

Words fail me to express my sincere thanks to my trusted companion: Miss Shittu Christiana to whom I am indebted for her all-round assistance.

I hereby wish to extend my thanks also to my covenant friends: Pastor Bode Esan, Pastor Emmanuel Musa, Miss Grace Twaki, Brother Kayode, Brother Ade, Brother Raphael, to the amiable Executive members of the Fellowship of Christian Students with whom I served for three tenures (97/98,98/99,99/2000); It will be impossible to forget you all and lastly to my colleagues and room mates for their friendliness and co-operation.

ABSTRACT

The Radio Frequency (RF) detector is of paramount importance in any work associated with radio frequency (RF) for the detecting and troubleshooting of radio frequency signals processing circuits.

Therefore, if any work is done at radio frequency (RF), the radio frequency detector is sure to be indispensable on the test bench. It can be used to tune and troubleshoot radio gears at frequencies ranging from the medium wave broadcast band to well within the ultra high frequency (UHF) region.

The report went on with the design and construction processes of the detector (RFD).

In the design analysis, the circuitry was made as simple as possible to aid reliability and understanding of the various stages of the system. It also shows the result obtained, the problems encountered, and conclusion and recommendations.

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CHAPTER ONE

INTRODUCTION

If any work is done with radio frequencies (RF), the RF detector is sure to be unavoidably utilised on the test bench.

The function of the RF detector is to tune and troubleshoot radio gear at frequencies ranging from the medium wave broadcast band to well within ultra high frequency (UHF) range.

The RF detector is broadly classified into four sections: The active probe section, the detector section, the amplifier section and the output transducer section.

Unlike most RF probes which simply uses a passive rectifier (detector) to read a signal into DC voltmeter, the unit has a FET broadband amplifier built into the probe tip and a variable gain sensitivity and lower loading signal (transmitter), thereby giving a high accuracy.

The RF signal from the active probe is fed into the detector, which converts it into DC voltage to the desired level, which is then fed into the output transducer section.

The output transducer is classified into two sections; they are the meter transducer and the audible transducer.

I n the meter transducer, conversion is made from analog signal to digital signal in order to allow easy reading of the output transducers.

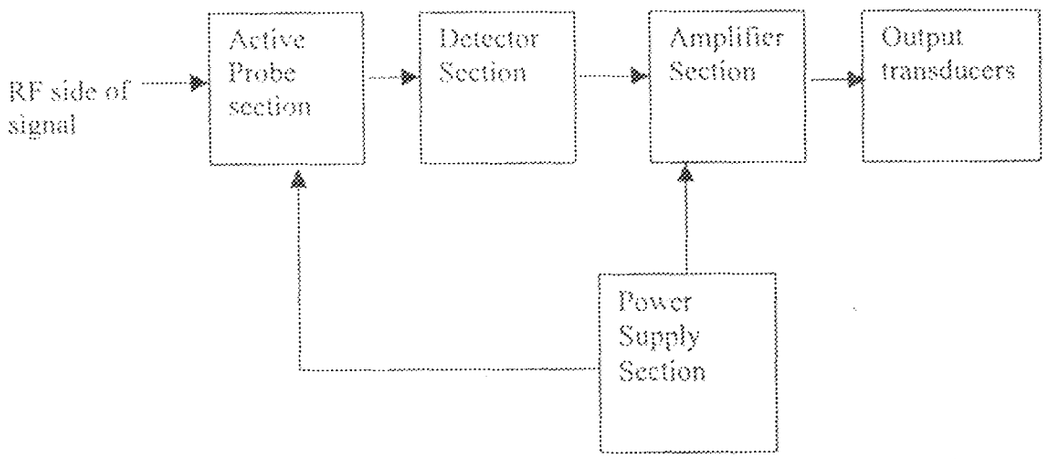

Fig 1.1 Block diagram of RF detector.

1.1 AIMS AND OBJECTIVES

The major aims and objectives of this research work was to make easier, the troubleshooting of radio equipment as well as compare transmitter antennas to overcome limitations in radio frequency radio circuit troubleshooting.

1.2 METHODOLOGY

The circuit of radio frequency detector is broken down into four sections: the active probe section, the detector section, the amplifier section and the output transducer section.

1.2.1 The probe section: The basic aim considered in the design of this section is radio frequency signal loading on the circuit of interest. The probe has a JFET broadband amplifier built into it. Junction Field Effect Transistors (JFET) are mainly used when it is essential that input resistance of the amplifier should be high. Its gate is held at zero voltage (0V) by the resistor (R1). The input impedance is high that the gate current is virtually

zero, by implication, the control terminal of the junction field transistor known as the gate requires no current and the potential difference across the resistor (R1) is zero voltage (0V).

1.2.2 The detector: The RF signal received and amplified is converted into pulsating DC voltage in this section. The process of recovering radio frequency signal (RF) is called detection, this is similar with half wave rectification. The diode is usually a point-contact type because its performance is much better at radio frequencies than that of the Pn junction power rectifier. The smoothing capacitor is much smaller because the frequency of operation is high.

1.2.3 The Amplifier section: The design of a suitable amplifier depends upon the transducer and the load, upon the required power output and upon the frequency or nature of the signal. The DC output of the detector is fed to the first half section of non-inverting input of a dual operational amplifier. The operational amplifier (OA) which was configured to perform DC amplification by appropriate external circuit (Circuitry that is not part of the amplification itself) using a variable feedback gain; whereby part of the output signal is fed back (or added) to the input signal of the operational amplifier. Through its continually variable gain, the circuit's sensitivity can be adjusted as required. The second half of the dual operational amplifier, functions as a comparator. The positive feedback part through a resistor (R8) within the output and non-inverting input produces a hysterises voltage allowing the amplifier's output to alternate between saturation and cut off. A second feedback loop is formed via resistor (R9) and a capacitor (C4), connected between the output of second dual operational amplifier and its inverting input.

1.2.4 The output transducer section: The output of the first half section of the dual operational amplifier is fed directly to an analog voltmeter section. The second half of dual operational amplifier output which function as a free running pulse generator are fed to a

piezo electric transducer, which produces an audible indication of (RF) radio frequency level.

1.3 LITERATURE REVIEW

The development of radio frequency detector started with the discovery of the radio wave (electromagnetic waves). The existence of radio frequency was predicted long before they were actually discovered. An English physicist; Ernest Rutherford (1871-1937) succeeded in sending signals ¾ miles and another English man: Oliver Logdge (1851-1940) developed the basic principle of detector. The modern detector system for detecting radio frequency signal has the following parts:

The probe: The input radio frequency signal, which may be in the analog or digital, must be converted from its original form into an electrical signal to enable it to be processed by the necessary electronic circuit.

The Amplification: This involves the processing of the desired signal received from the probe. The processing function includes conversion of selected signal to a form suitable for the output transducer, this include detection or demodulation (opposite of modulation) and amplification (voltage and/or power), if the received signal is low.

The output Transducer: This is an element or device that converts electrical signal from the probe into the form desired by the user, for instance, a piezo transducer converts electrical signal to sound wave for the user to hear. Among other common output transducers are: Tele-typewriter, meter (analog or digital), oscilloscope etc.

CHAPTER TWO

SYSTEM DESIGN

The design of the system involves the determination of values of the components that make up the various stages of the RF detector. The stages are: the Pr4obe section, the detector section, the amplifier section and the output transducer section as well as the power supply unit.

Below are the common terms and parameters used in the design

V_{GS} – Gate to Source Voltage

I_D – Drain Current

V_{DS} – Drain to Source Voltage

V_S – Source Voltage

R_S – Source Resistor

V_P – Pinch off Voltage

I_{DSS} – Saturated Drain Current

V_G – Gate Voltage

V_{GSQ} – Quiescent Gate to Source Voltage

I_{DQ} – Quiescent Drain Voltage

g_m – Transconductance

F_O – Resonant Frequency

(A) THE PROBE SECTION

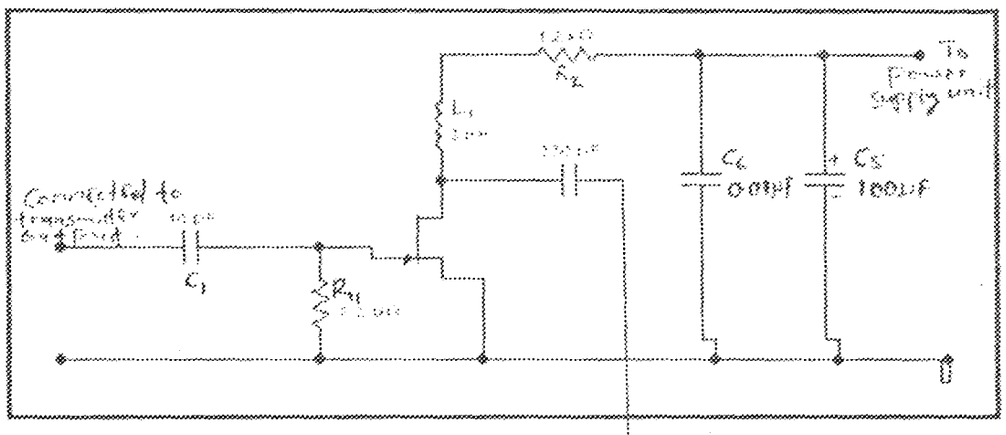

Fig. 2.1 The Probe Circuit diagram

To detector section

The analysis of these circuits involves device relationships, Shockley's equation and the circuit laws; KVL and KCL.

The purpose of the biasing circuits is basically to establish a desired V_{GSQ}, which results in a corresponding I_{DQ}. The analysis will then be concerned with the calculation of V_{GSQ} and I_{DQ} and is based on:

a) There is no gate current and the gate as well will be considered an open circuit.

b) Where I_D is approximately constant for a given V_{GS}, the Drain Source Voltage V_{DS} is assumed large enough for the transistor to be operating in the "pinch off " region.

The voltage supply from the source is passed through the combination of RF Choke (L_1) inductor and resistor R_3 to supply DC power to the probe, while the two capacitors C_5 and C_6 serve as to filter the voltage ripple from the voltage source.

The above circuit in fig 2.1 was reduced to the form shown below in fig 2.2 below.

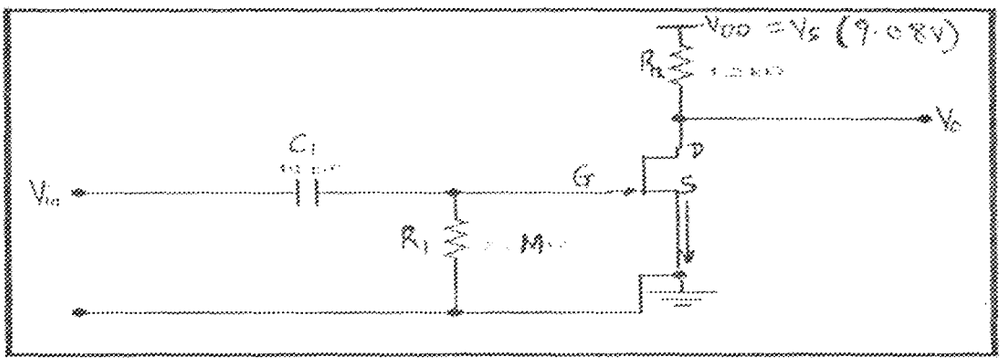

FIG 2.2 Amplifier Circuit of the probe section

Because the impedance of RF Choke (L_{11}) inductor is very low, therefore, the voltage drop across the Choke (L_{11}) inductor is negligible. Also the RF Choke (L_{11}) inductor act as an high impedance to incoming ac signal being amplified by the junction field effect Transistor (JFET).

To find the operating point, Q, KVL is applied to be the gate-source loop.

KVL applied to the input loop yields the general equation:

$$V_G - V_{GS} - V_S = 0 \quad \text{..... equ (1)}$$

Since $V_S = I_{DRS}$

$$V_G = V_{GS} - I_{DRS} = 0 \quad \text{..... equ (1)}$$

OR

$$V_{GS} = V_G - I_{DRS} = 0.$$

For $V_G = 0$ (there is no current passing through R_G, hence no voltage across it).

Therefore, $V_{GS} = -I_{DRS}$

From the circuit diagram, $R_S = 0$

$V_{GS} = 0$

$V_{GSQ} = 0$

To find I_{DQ}, Shockley's equation is used.

$I_D = I_{DSS}(1 - V_{GS}/V_P)^2$

The parameter given by the transistor manufacturer for BF 247 N channel JFET is given as follows:

$V_p = 6$ Volt

$I_{DSS} = 15$ mA

$g_m = 5500$

Therefore,

$I_{DQ} = 15 \times 10^{-3}(1 - 0)^2$ A

$I_{DQ} = 15 \times 10^{-3}$ A

$I_{DQ} = 15$ mA

A pair of resistors connected in series with inductor (L_1) and capacitor (C_2) (R_2 & R_3) respectively, helped to reduce the circuit's Q to prevent a large increase in response at the resonant frequency of C_2 and L_1.

$$F_o = \frac{1}{2\pi\sqrt{L_1 C_2}}$$

$C_2 = 330$pf $= 330 \times 10\text{-}12$ forced

$C_2 = 330 \times 10^{-6}$ micro farad (μf)

$L_1 = 3\mu H$

$$Fo = \frac{V}{2\pi\sqrt{L_1 C_2}}$$

$C_2 = 330 \times 10^{-12}$ f

$L1 = 3 \times 10^{-6}$ H

$$Fo = \frac{1}{2\pi\sqrt{13\times10^{-6}\times330\times10^{-12}}}$$

$$Fo = \frac{1}{2\pi\sqrt{990\times10^{-17}}}$$

$$Fo = \frac{1}{2\pi \times 3.1 \times 10^{-8}}$$

$$Fo = \frac{1}{1.94 \times 10^{-7}}$$

Fo = 5134030.422Hz

Fo = 5.134×10^6 Hz

Fo = 5.134MHz

$$Qo = \frac{Wo\ L1}{R\ d\ c} = \frac{2\pi\ Fo\ L_1}{R\ d\ c}$$

R d c = The integral resistance of the inductor

R d c = 0.8μ

Fo = 5.134 mf

= 5.134×10^6 F

L1 = 3×10^{-6} H

$$Qo = \frac{2\pi \times 5.134 \times 10^6 \times 3 \times 10^{-6}}{0.8}$$

$$Qo = \frac{2\pi \times 5.134 \times 3}{0.8} = \frac{96.77}{0.8}$$

Qo = 120.97

The half power frequency point for the resonant circuit are: for $Q_0 >> 1$

$$F_L = F_o\left(1 - \frac{1}{2Q_o}\right)$$

$$F_H = F_o\left(1 + \frac{1}{2Q_o}\right)$$

The broadwidth B is then given as the difference between the two half power frequencies.

$B = F_H - F_L$

$Fo = 5.134 \times 10^6 Hz$

$Qo = 120.97$

$$F_L = 5.134\times10^6\left(1 - \frac{1}{2\times120.97}\right)$$

$$F_L = 5.134\times10^6\left(1 - \frac{1}{241.94}\right)$$

$F_L = 5.134 \times 10^6 (1 - 4.13 \times 10^{-3})$

$F_L = 5.134 \times 10^6 \times 0.9958$

$F_L = 5.113 \times 10^6$ Hz

$$F_H = F_o\left(1 + \frac{1}{2Q_o}\right)$$

$$F_H = 5.134\times10^6\left(1 + \frac{1}{2\times120.97}\right)$$

$$F_H = 5.134\times10^6\left(1 + \frac{1}{241.94}\right)$$

$F_H = 5.134 \times 10^6 (1 + 4.13 \times 10\text{-}3)$

$F_H = 5.134 \times 10^6 \times 1.00413$

$F_H = 5.155 \times 10^6$ Hz

Bandwidth (B) = $F_H - F_L$

$B = 5.155 \times 10^6 - 5.113 \times 10^6$

$B = 0.042 \times 10$

$B = 42KHz$

$\Rightarrow$ Bandwidth = 42KHz

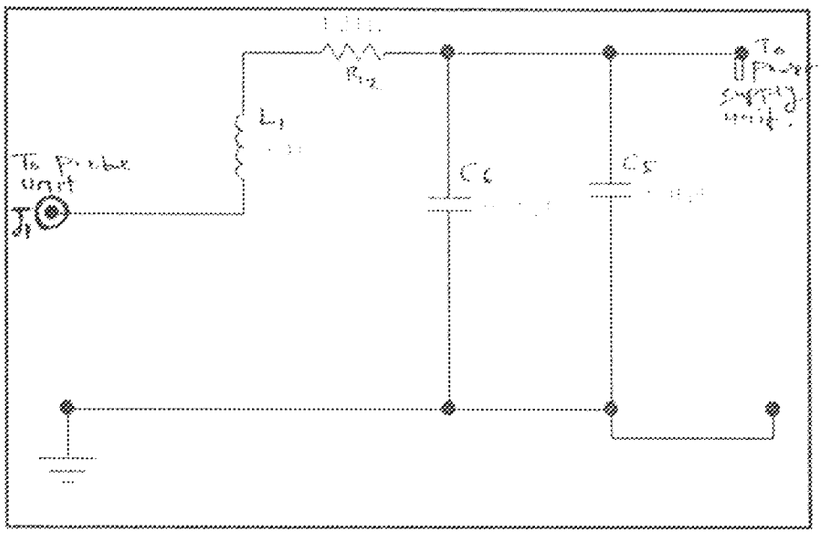

Fig. 2.3 DC Power Circuit

Fig 2.3 consists of an inductor (L_1) and R_2 which are in series with one another and also a parallel combination of both capacitors C_5 and C_6 all of which are connected to the main power supply.

$L_1 = 3$ µH

$R_2 = 1.2$ KΩ

$C_6 = 60$ µf electrolytic

$C_5 = 0.01$ µf ceramic disk

Both capacitors C_1 and C_2 are used as smoothing capacitors, the L_1 & L_2 combination supplies DC Power from the power supply unit to the probe, which serves as to power the JFET transistor, which is used as an amplifier

THE AMPLIFIER UNIT

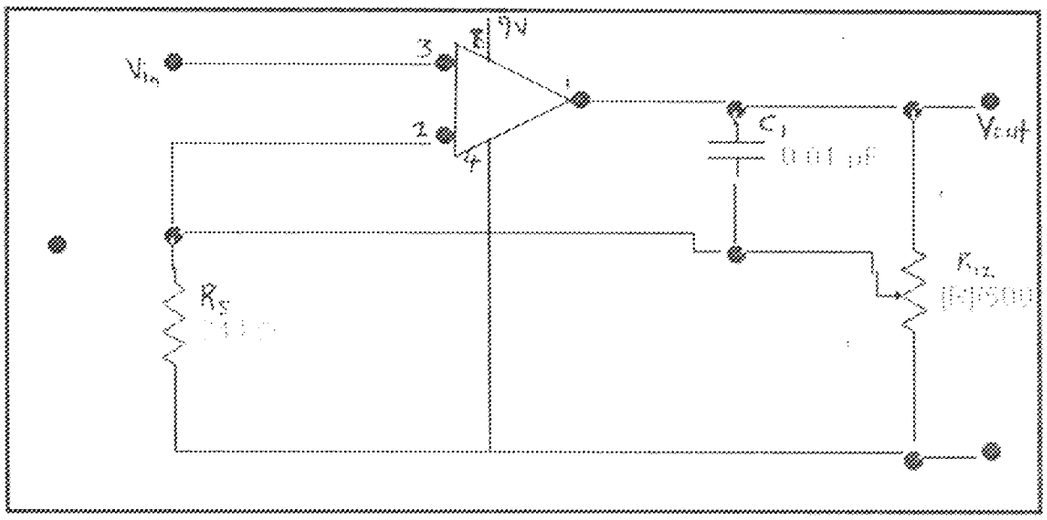

Fig. 2.4 Amplifier Circuit Diagram

The output of the detector is fed to the non-inverting input of IC, which is connected as a non-inverting amplifier. With a non-inverting amplifier, the input has to be applied to the plus (+) input but the feedback has to be applied to the negative (-) input.

CALCULATION:

The fraction of V_{out} sent to the inverting (-) in V_f where

$$V_f = \frac{V_{out} \times R_S}{(R_S + R_{VR})} \quad \text{.....(i)}$$

The voltage difference between the two inputs = V_i, where

$$V_i = V_{in} - V_f \text{ .....(ii)}$$

V_{in} is the voltage actually amplified by the Opamp.

Now: $V_{out} = A_o \times V_i$ .....(iii)

Where A_o is the open-loop gain of the Opamp.

Substituting for V_i in (ii), using (iii), then

$V_{in} - V_f = V_{out} / A_o$ and

$V_f = V_{in} - V_{out} / A_o$ ..... (iv)

Substituting V_f in (i) using (iv)

$$V_{in} - \frac{V_{out}}{A_o} = \frac{V_{out} \times R_5}{(R_5 + R_{12})}$$

$$V_{in} = V_{out} \left(\frac{R_5}{(R_5 + R_{12})} + \frac{1}{A_o} \right)$$

$$\text{Gain} = V_{out} / V_{in} = (R_5 + R_{12}) / R_5$$

Since A_o is typically about 10^5 and $1/A_o$ is negligible.

So the gain of this amplifier only depends on the value of variable resistor R_{12} (500 KΩ) and R_5 is dependent of the open-loop gain of the opamp.

Maximum Voltage Output = 1 + (500 KΩ / 24KΩ)

= 1 + 20.83

= 21.83

≈ 22 X V_{in}

V_{in} = Signal Voltage from any transmitter.

FREQUENCY RESPONSE OF THE AMPLIFIER UNIT OF THE CIRCUIT

The gain of an operational amplifier depends on its frequency; without a feed back that is; open loop gain. It drops rapidly from 105 at low frequencies to 1 at very high frequency. This situation is clearly not ideal since amplifiers generally require the gain to be constant at all frequencies. However, as the negative feed back increase and the overall gain becomes lower, the gain remains constant over a wider range of frequencies and so the frequency response of the amplifier is improved.

Since the operational amplifier circuit is a dc amplifier, its amplifier signal down to dc (zero frequency) and the band width of amplifier is given by the upper cut- off frequency function (in many data sheets is referred to as f_2)

The upper cut-off frequency for the amplifier with feedback can be obtained from the amplifier with feedback can be obtained from the cut – off frequency of the amplifier in the form:

$F_{2CL} = (1+\beta\ 1A1> x\ f_2$……………………(i)

Where f_{2CL} is the closed cut –off frequency and f_2 is the open loop (m0 feedback) cut –off frequency.

The closed loop gain can be calculated

$V_o = A \times V_{in}$

V_o = output voltage of the opamp.

V_{in} = input voltage of the opamp.

A = gain of the Opamp

β = a feedback of the opamp

$Vo = AV_{in} A (V_1 + \beta Vs)$……………………………………(2)

Solving, for V_0 we get

$Vo = AV_1/(1-A\beta)$………………………………… ……….(3)

And $V_o/V_1 = A_{Cl} = A/(1-\beta A)$ ……………………………..(4)

Since A is negative, that is A = -1A1.

1A1 is the magnitude of A and it is always positive

$A_{CL} = Vo/V1 = 1A1/(1+\beta 1A1)$………………… …………………(5)

$1+\beta A = A/A_{CL}$……………………………………………… ………(6)

So that equation (1) becomes

$F_{CL} = A/A_{CL} x F_2$ (7)

So that equation (1) becomes

$F_{CL} = A/A_{CL} \times F_2$ ..... (7)

The equation (7) shows that the Band width is increased by the same proportion that which the gain is decreased.

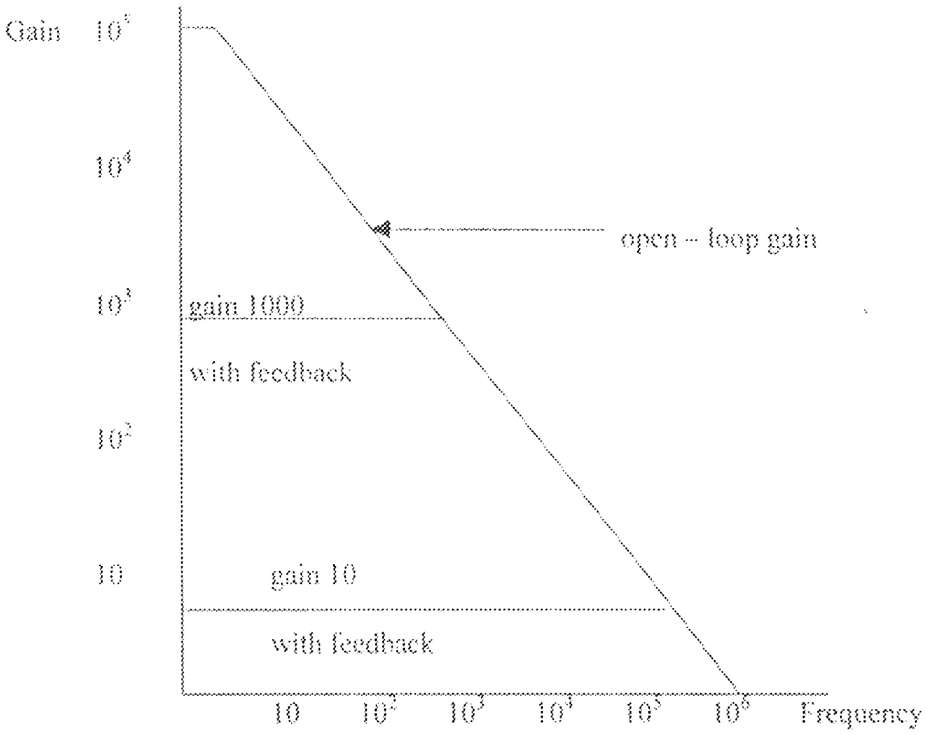

Figure (2.4.5) Frequency response of opamp circuit

THE PULSE GENERATOR UNIT

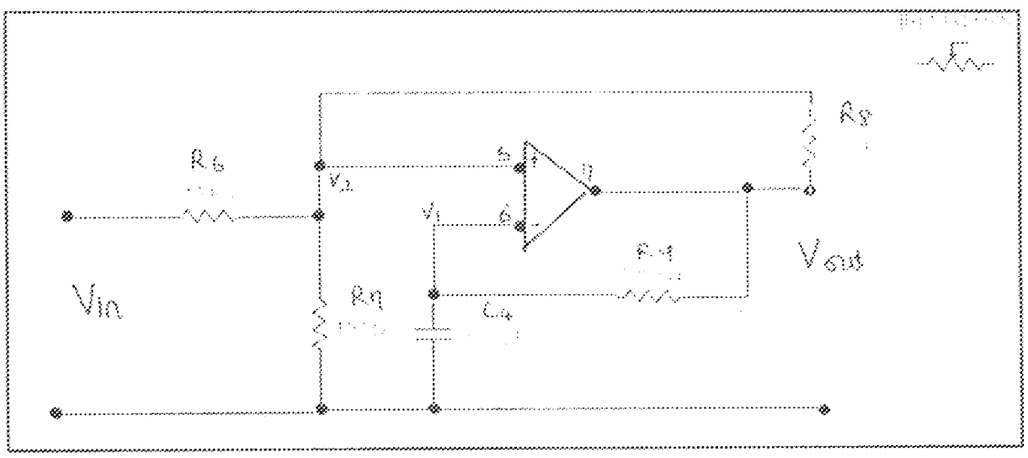

FIG 2.5 PULSE GENERATOR CIRCUIT DIAGRAM

inverting) input, any change in the output will tend to increase the differential voltage at the input, since the output voltage will be in phase with the input voltage. The output voltage will then quickly reach the saturation voltage; + V_s which is the supply voltage. If the opamp circuit is designed to make the output switch continually from + V_s to - V_s and from - V_s to + V_s an oscillating output voltage is observed.

To explain the action of this circuit, suppose the capacitor C_4 is initially uncharged and that the output voltage V_{out} has its maximum positive value (+V) due to a small differential voltage at the inputs. A fraction (V_2) of V_{out} is fed back to the non-inverting input.

$V_2 = (V_{out} \times R_7) / (R_7 + R_8)$

$V_{out} = ?$

$R_7 = 10K\Omega$

$R_8 = 100K\Omega$

The voltage V_1 is the voltage across the capacitor C_4 of 0.02μf, which is in series with the resistor R_9 (100KΩ) across the voltage out.

The time constant of the circuit $= C_4 \times C_9$

$C_4 = 0.02\ \mu f$

$R_9 = 100\ K\Omega$

$C_4R_9 = 0.02 \times 10^{-6} \times 100 \times 10^{3}$

$C_4R_9 = 0.002$ s

$C_4R_9 = 2$ ms

$\Rightarrow \quad V_1 = V_{out}(1 - e^{-t/CR})$

$\Rightarrow \quad V_1 = V_{out}\,(1 - e^{-t/CR})$

$t = 12.18$ ms

$C_9 = 2$ ms

$V_1 = V_{out}\,(1 - e^{-12.18\,/\,2})$

$= V_{out}\,(1 - e^{-6.09})$

$= V_{out}\,(1 - 0.00227)$

$V_1 = V_{out}\,(0.998)$

$V_2 = (V_{out} \times R_7) / (R_7 + R_8)$

$= (V_{out} \times 10\ K) / (10\ K + 100K)$

$= (V_{out} \times 10\ K) / (110\ K)$

$V_2 = 0.09 \times V_{out}$

$= 0.09V_{out}$

But V_{out} is also fed back into the inverting input through R_9, so C_4, which is initially uncharged, starts to charge up through R_9 towards +V and the voltage V_1, then rises exponentially with time. After a time, which depends on the time constant.

Time constant = $C_4 \times R_9$

$C_4 = 2200$ pf = 0.02 μf

$R_9 = 100$ K

$= 0.02 \text{ X } 100 \text{ x } 10^{-3}$s

$= 2 \text{ x } 10^{-1}$s

Time constant = 2s

V_1 reaches a value higher than V_2, whereupon the output of the Opamp switches over so that the output is –V. The positive feedback encourages the Opamp to switch quickly since V_2 then drops, making V_2 much lower than V_1 and so forcing V_{out} to go negative even more quickly. C_4 now discharges and starts to charge in the opposite direction until V_1 becomes lower than V_2

The cycle is then repeated, in essence, this unit functions as free running pulse generator.

The periodic time of the pulse generator is given by:

$T = 2C_4R_9ln(1+2R_8/R_7)$

$C_4 = 2200pf = 0.02\mu f$

$R_9 = 100k\Omega$

$R_8 = 100k\Omega$

$R_7 = 10k\Omega$

$T = 2 \text{ x } 0.02 \text{ x } 10^{-6} \text{ x} 100 \text{ x } 10^{-3} \ln (1 + 2 \text{ x } 100 \text{ x } 10^3 / 10 \text{ x } 10^3)$

$= 2 \text{ x } 0.02 \text{ x } 100 \text{ x } 10^{-3} \ln (1 + 2 \text{ x } 100/10)$

$= 4 \text{ x } 10^{-3} \ln (21)$

$= 4 \times 10^{-3} \times 3.0445$

$\approx 4 \times 10^{-3} \times 3.045$

$\approx 12.18 \times 10^{-3}$

T = 0.01218 s.

Frequency = 1/T

Frequency f = $\frac{1}{12.18 \times 10^{-3}}$

F = 82.1018

F= 82Hz

DETECTOR SECTION

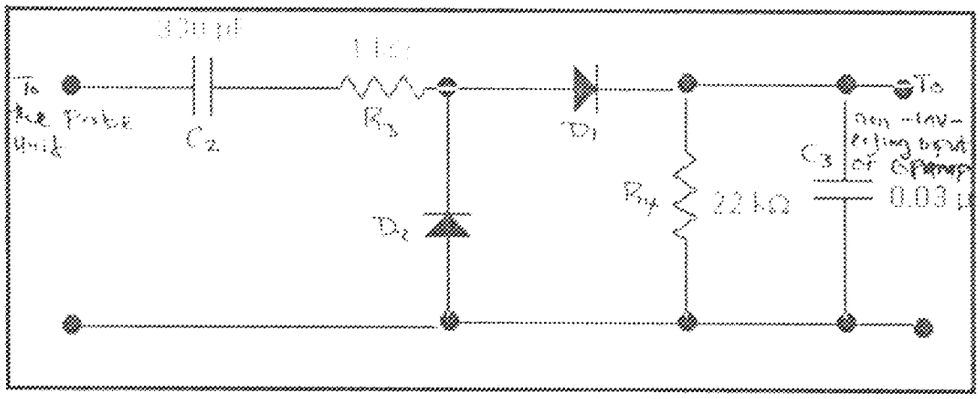

Fig. 2.6 Detector Circuit Diagram

Fig 2.6 above consists of signal-detectors D_1 and D_2 (1N60), Resistor R_3 and R_4 and capacitors: C_2 and C_3 for the RF signal to be reconstructed without much error, the filter stage which consist of R_4 and C_3 must obey the inequality as stated below.

$1/F_C << R_4C_3 << 1/w$.

Where F_C is the carrier frequency (Radio frequency (RF)) and w is the band width of maximum frequency of the message signal.

The time constant of the filter is given as:

R_4C_4= time constant (t).

R_4=22k

C_3=3300pf

$t = 22 \times 10^3 \times 3300 \times 10^{-12}s$

$= 72600 \times 10^{-9}s$

$t \approx 0.0726ms$

$t = 72.6\mu s$

The components capacitor C_3 and resistor R_4 are used to couple the radio frequency RF signal to the detector (comprised of D_1&D_2). The detector converts the radio frequency (RF) signal to a DC voltage, which is fed into non-inverting input of Opamp.

(D) OUTPUT TRANSDUCER.

The can be classified into two major parts as follows: The meter display and the audible indication of RF level.

These serve as to display or indicate the radio frequency (RF) signal, which is being detected through the probe section and amplified.

METER DIPLAY

The output of IC_1-a is fed directly to the meter display or the output of IC_1-a can be fed to a pair of jacks, allowing the circuit to feed an analog voltmeter (AVM) to indicate the reading of radio frequency (RF) output signal, which was detected.

This voltmeter consists of a permanent magnet, moving coil pivoted on jewel bearings, control springs and a point test.

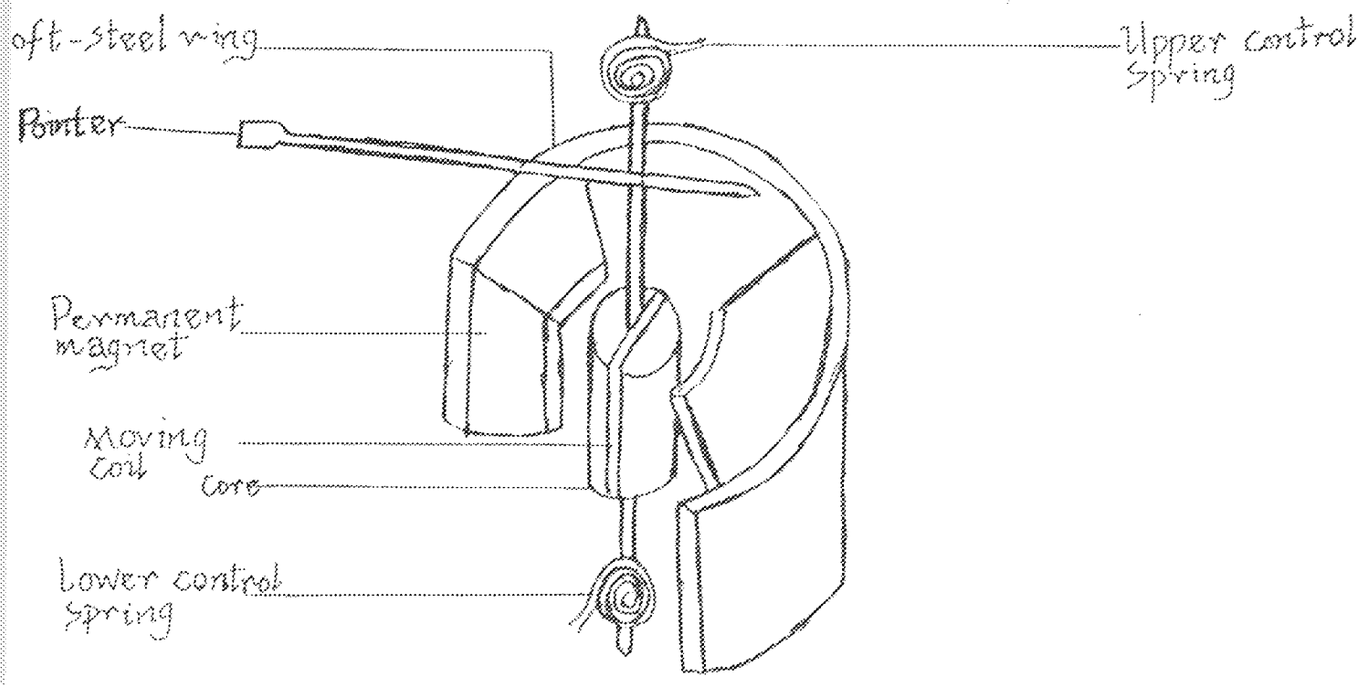

Fig. 2.7 Moving Coil Voltmeter

Current I is passed through the moving coil of N turns via the two control springs which apply a restraining torque Te equal to KS0, where Ks is the spring constant and 0 is the angle of deflection.

The deflection torque Te is equal to the product of the magnetic moment of the coil and the field intensity B.

Te = NIWLB.

Where W and L are coil width and length respectively. The deflection θ resulting from the current I is given by $\theta = BNIWL/K_S$

AUDIBLE INDICATOR

The audible indicator of radio frequency (RF) detector is bult around ICl-b, which function as a comparator. The output of the comparator which functions as a free running pulse generator is fed to a piezo electric transducer (TD1) which provides an audible indication of radio frequency (RF) level yielding a notable sound.

(E) POWER SUPPLY SECTION

The unit consist of the transformer, bridge rectifier, fitter capacitor and fixed voltage regulator integrated circuit (IC).

(i) TRANSFORMER: The transformer used is a step down transformer, of 220V/12V rating.

(ii) BRIDGE RECTIFIER: This does not require a special transformer but requires for diodes. On each half cycle, two diodes are conducting while two are non-conducting. The bridge can be made by connecting four individual diodes but it is easier to use a bridge rectifier which is ready made device with the four diodes connected inside it. Fig. 2.8 below shows the full wave rectifier using a bridge of four diodes and its output waveform.

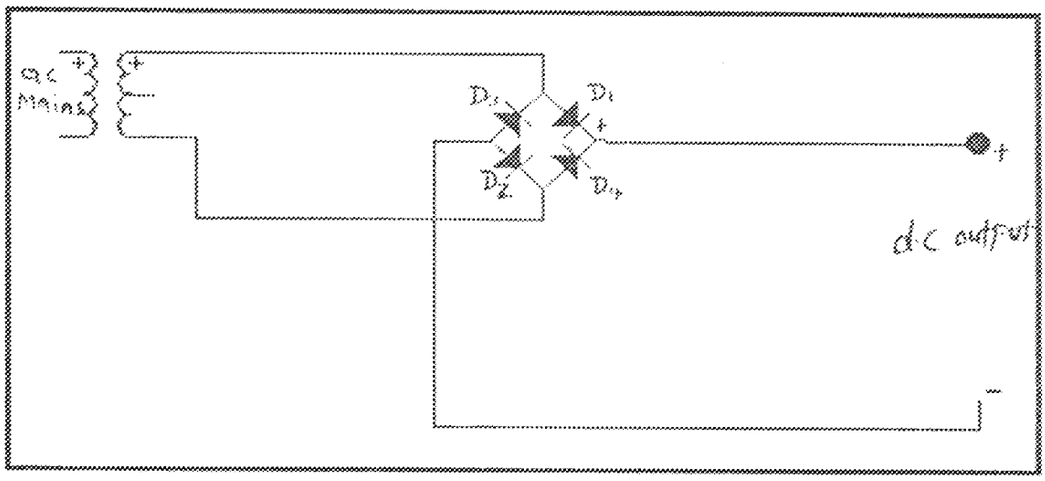

Fig. 2.8 (a) Full-wave rectifier using a bridge of four diodes.

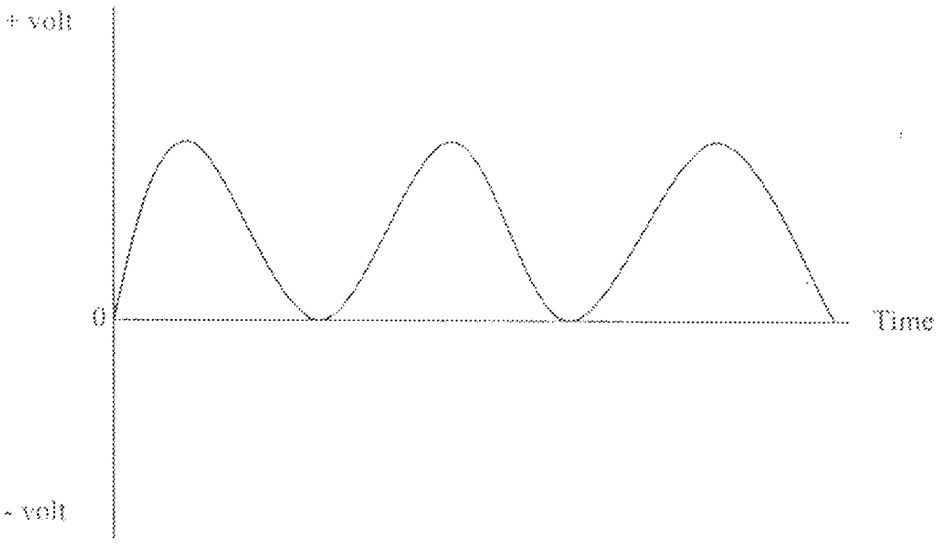

Fig. 2.8 (b) The output waveform.

It is advisable where designing a rectifier, the peack inverse voltage (PIV) of which device must be taken into account and it is the greatest reverse potential difference that the diode which is not conducting needs to withstand if Erms of the secondary is 12V, the PIV is from

$E_{peak} = V_m \times E_{rms}$

E peak = 12 x $\sqrt{2}$ = (12 x 1.414)

E peak = 16.970.

(iii) FILTER CAPACITOR: The fig 3. below shows a full wave rectifier with a filter capacitor. The capacitor stores energy during the conduction cycle of the diodes and delivers energy to the load during the non-conducting cycle.

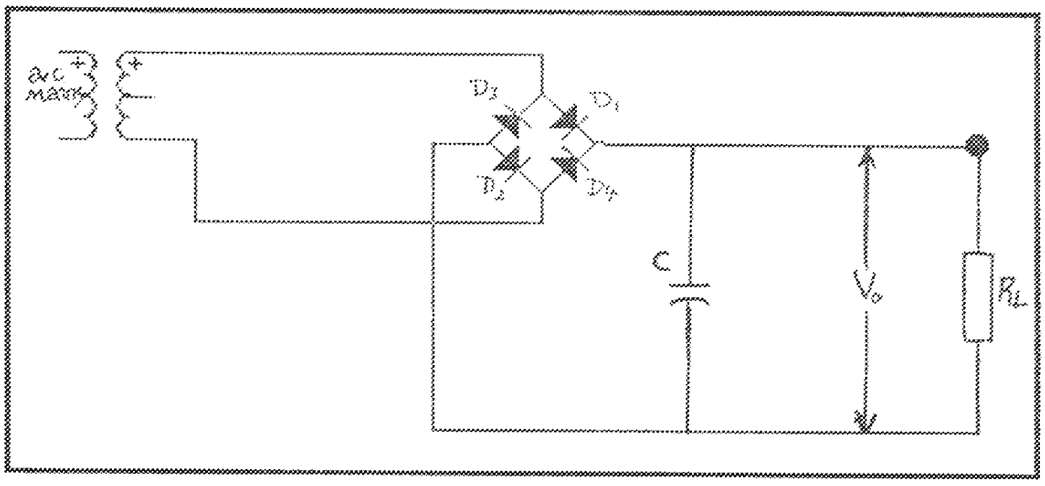

Fig. 2.9 (a) Full – wave rectifier with a capacitor filter

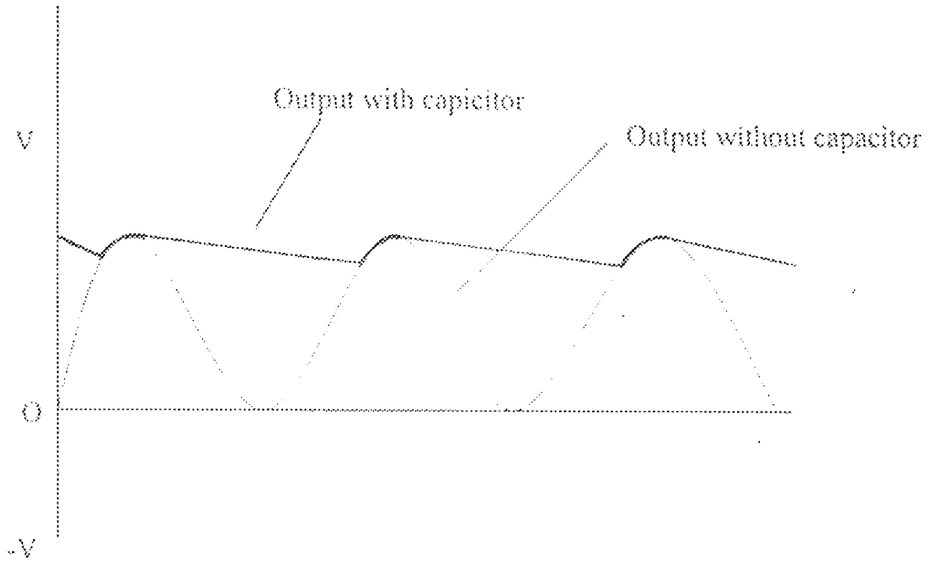

Fig 2.9 (b)

Fig. 2.9 (b) Approximate output voltage of capacitor filter for a full – wave rectifier

Hence there is always current passing through the load, which considerably reduces the ripple. If RC = T, where T is the period of the input ac signal, then the load voltage and current will have a low ripple in their wave form. An approximate analysis indicated in fig 3.8 (b) provides reasonably accurate results when the ripple factor is small. This analysis for full wave rectification ripple.

$$V_{dc} = \frac{V_M}{1 + 1/4FR_LC} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(i)$$

$$r \text{ (ripple factor)} = \frac{1}{4/\sqrt{3}\ FR_LC} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(ii)$$

$$\text{ripple voltage } V_r = \frac{V_m}{2FR_LC} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(iii)$$

Where F is the frequency of the input ac signal. Note that the magnitude of the ripple voltage Vr varies inversely with the time constant R.C and any charges in the load current cause changes in the ripple voltage. As the load current increases, the DC output voltage decreases considerably. Therefore, the voltage regulation of the capacitor filter is very poor.

(iv) FIXED VOLTAGE REGULATOR: 78XX series terminals positive fixed voltage regulators. In 78XX, the last two numbers (09) indicate the output voltage.

Fig 3. shows standard representation of a monolithic voltage regulator. A capacitor C2 is usually connected between input terminal and also between output terminal and ground.

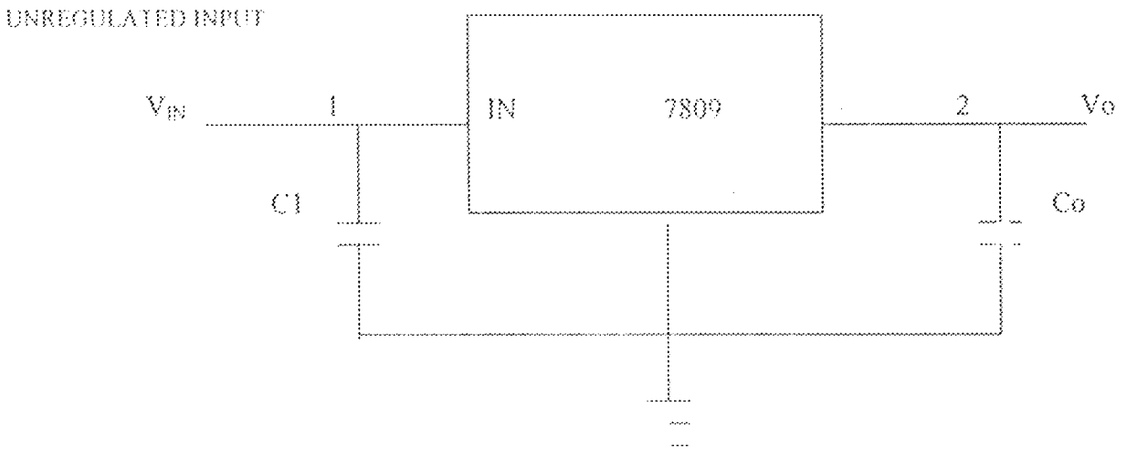

Fig. 2.10 Monolithic voltage regulator representation.

CHAPTER THREE

3.0 CIRCUIT CONSTRUCTION

The circuit construction started with the schematic layout of components on paper, which after being checked and crosschecked was transferred to the breadboard according to the design.

After the arrangement on the breadboard was completed it was crosschecked again to ascertain that there was no mistake before it was connected to oscilloscope for testing.

Consequently, the RF detector was assembled in two parts. The first part comprised of the active probe while the second part was made up of the detector, amplifier and the output transducer.

The probe was built into the body of an old tempo pen; the three parts were wired to the end of a length of a cable and pushed through the tempo pen. The probe is comprised of BF274 high – frequency junction FET, a 2.2- mega ohms or resistor R_1 and capacitor C_1.

The free end of capacitor C1 was soldered to a probe tip. A wire small enough to squeeze through the hole in the tempo pen was used as the ground wire.

After the assembly was installed in the burred of the tempo pen, a small alligator clip was connected to the free end of the ground wire.

To insert the probe tip, heat was applied through soldering, which was pushed slowly to the tempo pen and allowed to cool. The free end of the probe`s main wire was connected to a male BNC connector.

The mating – Female BNC connector was then attached to the project's enclosure.

The second part of the RF detector was assembled on a Vero board including the detector, amplifier and digital part, and solder effectively.

The detector amplifier comprised of LM358IC which served as dual operational amplifier with external circuit connection being made which are:

R5,R6,R7,R8,R9,R10,R12,C4 and C7.

The output piezo transducer was used and it served the purpose of indicating the Level of RF detector by sound indication

3.1 TESTING

Each stage was tested as soon as they were completed and the wave form Observed, using oscilloscope, the results obtained were:

(i) It was observed that signal was picked up by the probe section when used to test the front and of (RF). Radio frequency transmitter, by implication, the picked signal was being amplified to broadband gain.

(ii) The combination of AC signal was also observed.

(iii) It was observed at the output of detector that the radio frequency signal was converted to a DC voltage.

(iv) It was observed that the signal amplified at the amplifier stage was non- inverting.

(v) A free running pulse generator was observed at the output of amplifier stage 2.

(vi) It was inclusively observed that as the DC input bias to the circuit increase, the width of the gap between the two trip points narrows and the frequency of the pulse generator increases.

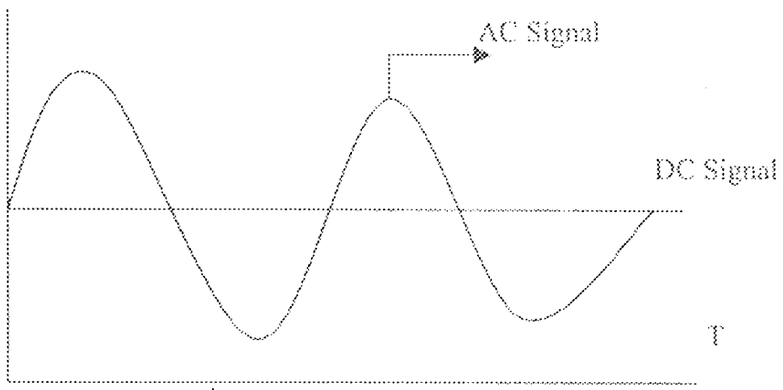

Fig 3.1 output of the Probe stage

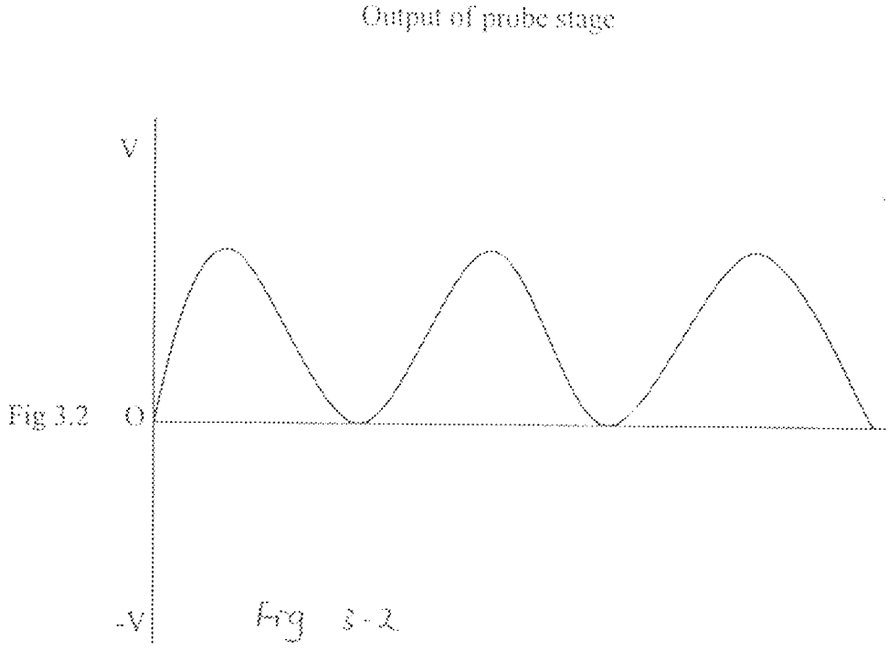

Fig 3.2

Fig 3-2

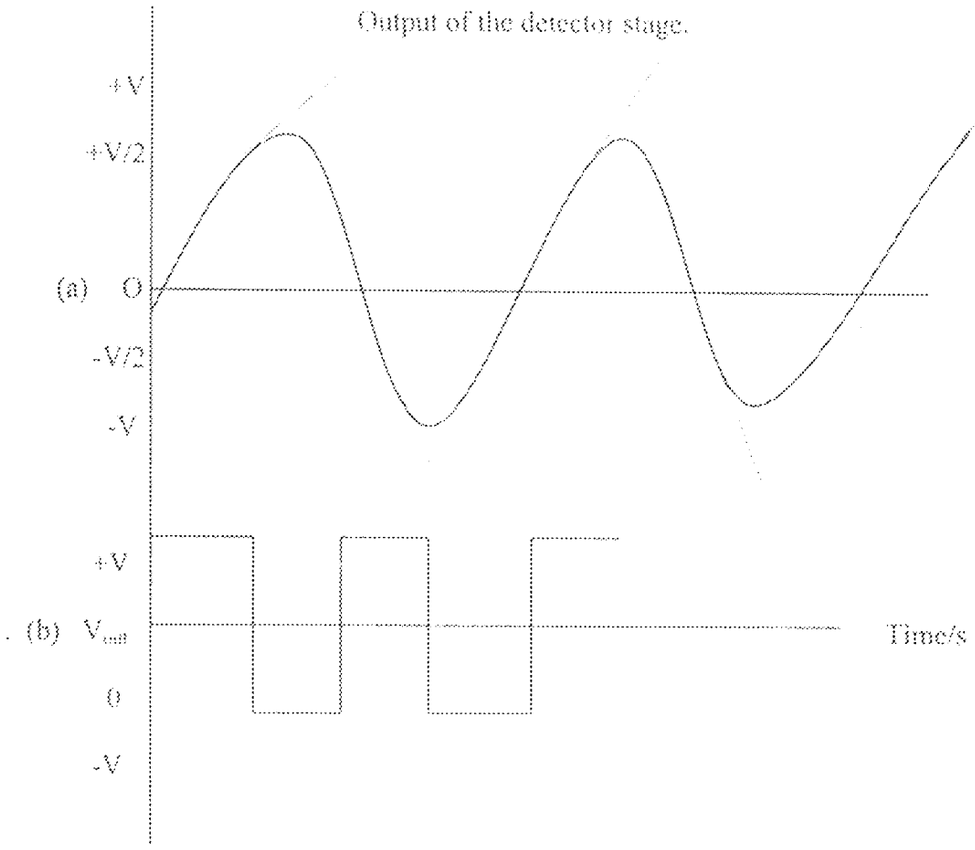

Fig 3.3 (a) variation of V_1 with time

Fig 3.3 (b) variation of V_{out} square wave

3.2 DISCUSSION OF RESULT

The results were fairly in line with the expected outcome.

The probe was designed to reduce radio frequency (RF) loading on the circuit of Interest, which also provides broadband gain.

The combination of inductor (L1) and resistor (R2) was also designed to supply DC power to the probe, which is superimposed on the output AC signal from the probe junction in fig 3.1.

The components capacitor (C_2) and resistor (R_3) are used to couple the radio frequency (RF) signal to the detector (comprising of D_1& D_2).

The detector converts the radio frequency (RF) SIGNAL TP A dc voltage in fig 3.2

In fig 3.3, supposing that amplifier stage 2 (IC_{1-b}) had just gone high that causes capacitor (C_4) to charge through resistor (R_9) until voltage on it (and at the inverting input of (IC1-b) exceeds the voltage at the non-inverting input. That causes IC1-b output to uggle low, bringing non-inverting input (pin 5) of IC1-b. the lower hysteresis.

Capacitor (C_4) begins to discharge, until the voltage on inverting input (pin6) of IC1-b dropped to the level at non-inverting input (pin5) of IC1-b. these function as a free running pulse generator. As the DC input bias to the circuit increase, the width of the group between the two trip points (hysteresis voltage) narrows and the frequency of the pulse-generator increases. The output pulse are fed to a piezo electric, TD 1, which provides an audible indication of RF Level.

CASING:

The casing of the RF detectors system was based on the size of fabricated components. The designed construction was based on the size of transformer, piezo transducer, and the length of fabricated components and to accommodate the power supply unit. A wooden casting (plywood) was dimension as described: -

Length: 20cm

Breath: 15cm

Height: 15cm

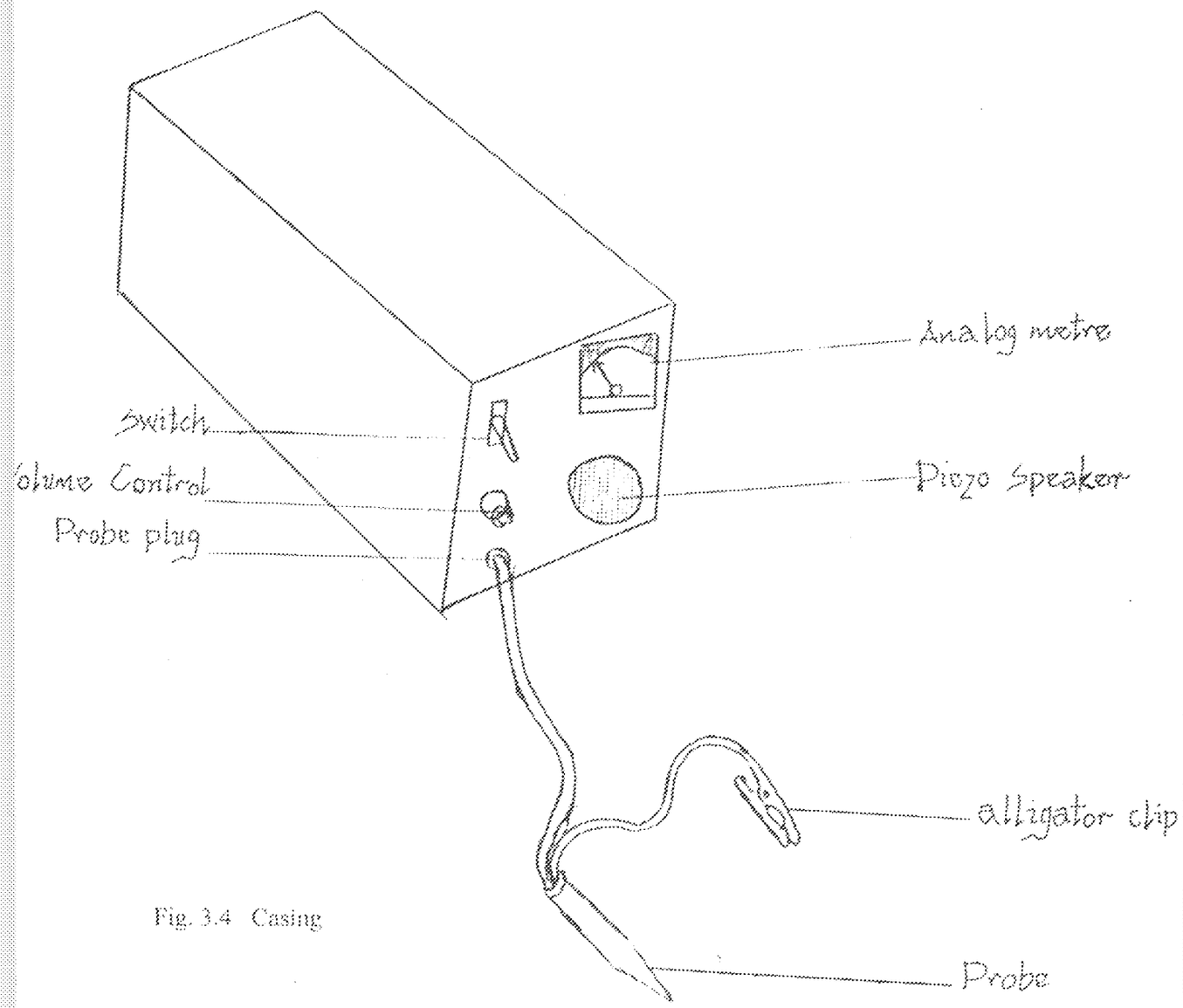

Fig. 3.4 Casing

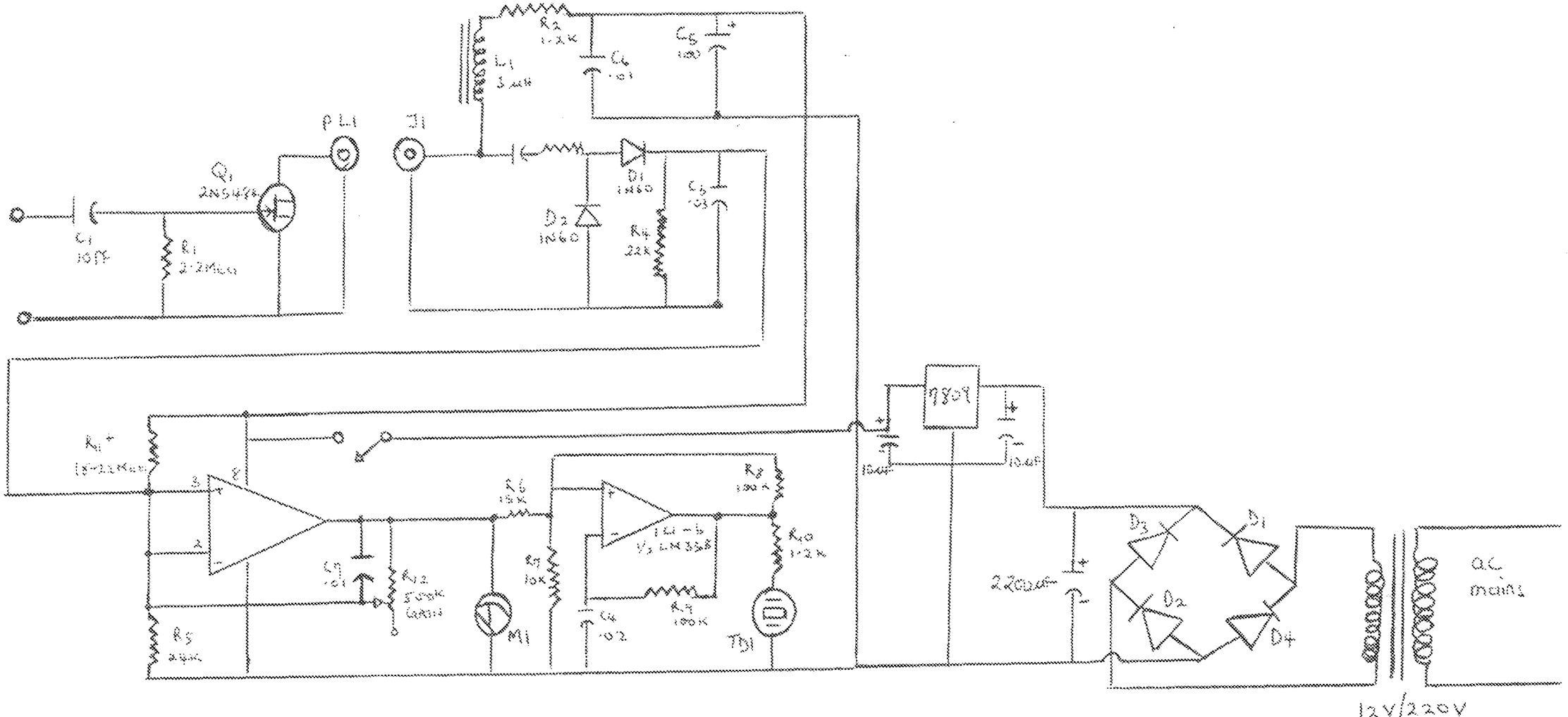

Fig 3.5 Complete Circuit diagram of the RF Detector

CHAPTER FOUR

CONCLUSION.

The system RF detector performed fairly well to expectation though with some associated level of distortion in the output.

The system was put into test and used to detect a relative field strength of a transmitter antenna which yields a level of RF indication by analog meter and also by audible transducer with an audible indication RF level.

4.1 LITARY OF PROBLEMS ENCOUNTERED

The design and the construction of radio frequency (RF) detector was successfully carried out as described.

In this design, the experimenter spent a lot of time trying to adjust and readjust before finally attained a satisfactory design.

A problem encountered was how to get the components. Although they were not expensive, yet most of them were scarce. Also, many of the calculated values of the components were not readily available; hence the ones with close values were used.

During the construction, another problem encountered was the construction of the probe junction; it was actually difficult for the probe to sniff in radio frequency signal from the transmitter whose output was not detected until proper troubleshooting was made.

Another problem tackled in the design was the pulse generator stage that is due to the charging and discharging of the capacitors to yield the accurate free running pulse generator frequency.

Finally, the major consideration in the casing was the length and the size of the fabricated components and a local source material (plywood casing) with this; a described dimension was used to reduce cost and to make the system portable.

4.3 RECOMMENDATION

Any student embarking on a similar project or carrying out the same research work, should incorporate the digital display instead of the analog to the system and such an individual should have a good background in the knowledge of electronic communication as this help a lot.

Care should be taken when choosing a place of industrial attachment to go to places that are of relevant importance to the project as this will expose him to the equipment to use.

It is very important for School of Engineering to provide necessary equipment for Electrical department, if not, the problem of lack of equipment will continue to affect the teaching of Electrical courses generally.

Conclusively, the department should be equipped with testing and construction equipment, instead of the students travelling to carry out a small work test, they could do it all in school. More so all the design and constructions should be properly kept for comprise of performance, reference and guides for incoming students at a later time.

4.4

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