DESIGN AND CONSTRUCTION OF PROGRAMMABLE TIMER

BY

ADAMA SIMEON SALA

97/5895EE

ELECTRICAL/COMPUTER ENGINEERING DEPARTMENT,

SCHOOL OF ENGINEERING AND ENGINEERING TECHNOLOGY,

FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA.

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DECLARATION

I, ADAMA SIMEON SALA, hereby declare that this is my original work, done under the supervision of Engr.M.D ABDULLAHI, and that it has not been presented wholly or partially elsewhere for any purpose. However, all previous works quoted are duly acknowledged.

STUDENT'S SIGNATURE

DATE

CERTIFICATION

This is to certify have I, have supervised, read, and approved this project work and is found to be adequate for the partial fulfillment of the award of Bachelor of Engineering in Electrical/computer (B.Eng).

STUDENT'S SIGNATURE — DATE: 16th Oct. 2009.

ENGR.M.D ABDULLAHI
(SUPERVISOR'S SIGNATURE) — DATE: 23/10/09

DR.Y.A ADEDIRAN
H.O.D's SIGNATURE
(ELECTRICAL/COMPUTER DEPT.) — DATE

EXTERNAL EXAMINER's
SIGNATURE — DATE

DEDICATION

This is dedicated to my parents; MR JOEL S. ADAMA and lovely mother MRS. RACHEL W. ADAMA.

ACKNOWLEDGEMENT

First, with much gratitude to the almighty God, the father of my Lord Jesus Christ who has made it possible for me at all academic levels up to this present level.

My great appreciation also goes to my parents for their relentless and sacrificial efforts to meet my needs as God provides for them. I am so grateful to them for laying this foundation for my future.

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I also want to thank all my Lecturers who taught me throughout the course of my study.

My words of acknowledgement will not be complete if I fail to appreciate my understanding uncles and aunties who have contributed in one way or the other to the success of my academic pursuit most especially Mrs. Mary Jiya and Dr. John Y. Adama.

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on whose computer I did most of my typesetting work. My appreciation also goes to GODWIN ABOH, my colleague in this project work.

Finally, I very much appreciate my friends and relations, F.C.S. F.U.T, Minna for their support and encouragement. Of course, I should not forget SEUN AJAGBE for his kind assistance and help.

ABSTRACT

This project is based on the design and construction of a programmable timer. The timer provides control to manufacturing processes on exact timing bases. This is required where human supervision may be difficult or critical to successful operation.

The idea behind this project emanated from a realization of the limitations and problems faced by the domestic and industrial sectors in this area over the years.

This project is based on the use of quartz crystal as clock generator for generating sequential clock pulses which are counted using down counters.

The expected result was achieved in the end as the relay switches off the machine at the maximum count down to zero that is logic signal 0000.

TABLE OF CONTENT

CHAPTER ONE

1.1: INTRODUCTION

The title of this project is "Design and construction of programmable timer ".

The timer is intended to provide control to processing or manufacturing events, appliances on an exact timing base. This can be used both at home and industry where the measurement of time and time –interval control are critical to successful operation without human supervision.

The construction of the timer is divided into categorically six parts. These include: The power supply unit (psu), the clock generator, the counters, the seven segment display unit , the control unit, and the relay unit.

The power supply unit deals with supply of 9V dc from common batteries to yield the low voltages needed by the crystal. The batteries convert the chemical energy to electrical energy in order to power the circuit.

The clock generator is intended to generate clock-pulses. The crystal – controlled clock generator used employ highly stable and accurate component called quartz crystal .It produce oscillations at an accurate and stable frequency equal to the crystal's resonant frequency. This particular clock generator was chosen because of the stability of its output frequency compared with Schmitt-trigger oscillator and 555timer e.t.c.

The seven-segment display unit covers the display of binary numbers as decimal characters. The seven-segment display consists of seven lines, which are connected in common-cathode. The display of binary numbers as decimal characters, .is done by BCD-to-decimal decoder/drivers. It is used to take a four – bit BCD input and provide the outputs that will pass current through the appropriate segments to display the decimal digit.

The counters are design to work on the principle of connecting a separate set of decoders/drivers and displays to each counter rather than multiplexing technique. The counters used are down counters (asynchronous or ripple counters), they count from a maximum count to zero in this project. Down counters are most suitable for this particular project since it is desired to know the number of input pulses that has occurred.

The control unit consists of logic gates in form of ICs, S-R Latch and switches. The major function of this unit is to preset the counters to any desired starting count asynchronously (independent of the clock signal).

The relay unit covers the execution of control operation. The task is executed when the 8-input NOR-gate /sensor indicates that the preset number of pulses has occurred to enable relay switch off. The relay pulls switch contact open when a control current pass through the coil and an electromagnet is formed. Also included here is the transistor driver circuit, used for switching to control direct current logic levels.

All the parts that shall be discussed in this write-up are done such that, it will be understandable by a layman.

The components used have been chosen for their credible accuracy and efficiency.

1.2: LITERATURE REVIEW

Over the years, numerous models of timer devices have been used by man to achieve a reliable and accurate time reference base for scheduling one or more domestic and industrial events with reference to time. However, with man's quest to make life more comfortable and safe, effort is being made to move from old methods to inventing best techniques.

The earlier means used include spring-timers (in an a alarm clock), fluid dash –pots, pneumatic devices, flea-power air motors, bimetallic devices e.t.c

However, the technology advancement in this era has brought about situations in industries where time- interval controls are critical to the successful execution of certain operations which may not permit human intervention or supervision hence, programmable timers will play vital roles in controlling such events.

This project's principle of the timer design is based on the application of counting pulses generated by means of quartz crystal which vibrates (resonates) at a frequency of 32.768KHZ which is divided by a 14- stage.

ripple carry binary counter /divider /oscillator (4060B IC) to give a clock pulse at two pulse per second and is again divided by a flip-flop. The relay triggers automatically when the preset number of pulses has occurred to switch off the desired system.

The design of this project in another trend using down counters, which will count down from a maximum count to zero instead of widely, used up counters.

CHAPTER TWO

2.0: ANALYSIS AND DESIGN OF COMPONENTS

2.1 PRINCIPLES OF OPERATION

The timer uses one of the common applications of counters, which count clock pulses coming out of a pulse generator at frequency of 1hz (i.e. one pulse per second; 1pps). This clock signals are generated by a highly stable and accurate component called a 'quartz crystal', which vibrates (resonate) when excited at precise frequency; this operating frequency (32768hz) is then divided by a frequency divider/oscillator (40603 IC) and flip-flop to give 1pps.

The clock pulse generator at frequency of 1hz(i.e.one pulse per second) is fed into aMOD-10-counter (decade counter) of the SECOND section which counts and displays seconds from 59 through 0 . The MOD-10-counter output recycles every 60s.

The same signal isfed to the MINUTE section, which count and display minute from the maximum preset minute through zero.

The relay unit trigger automatically, at the end of 0000 count of the maximum preset count to switch off the system.

The block diagram of the principle of operation of the timer is shown in figure 2.0 below.

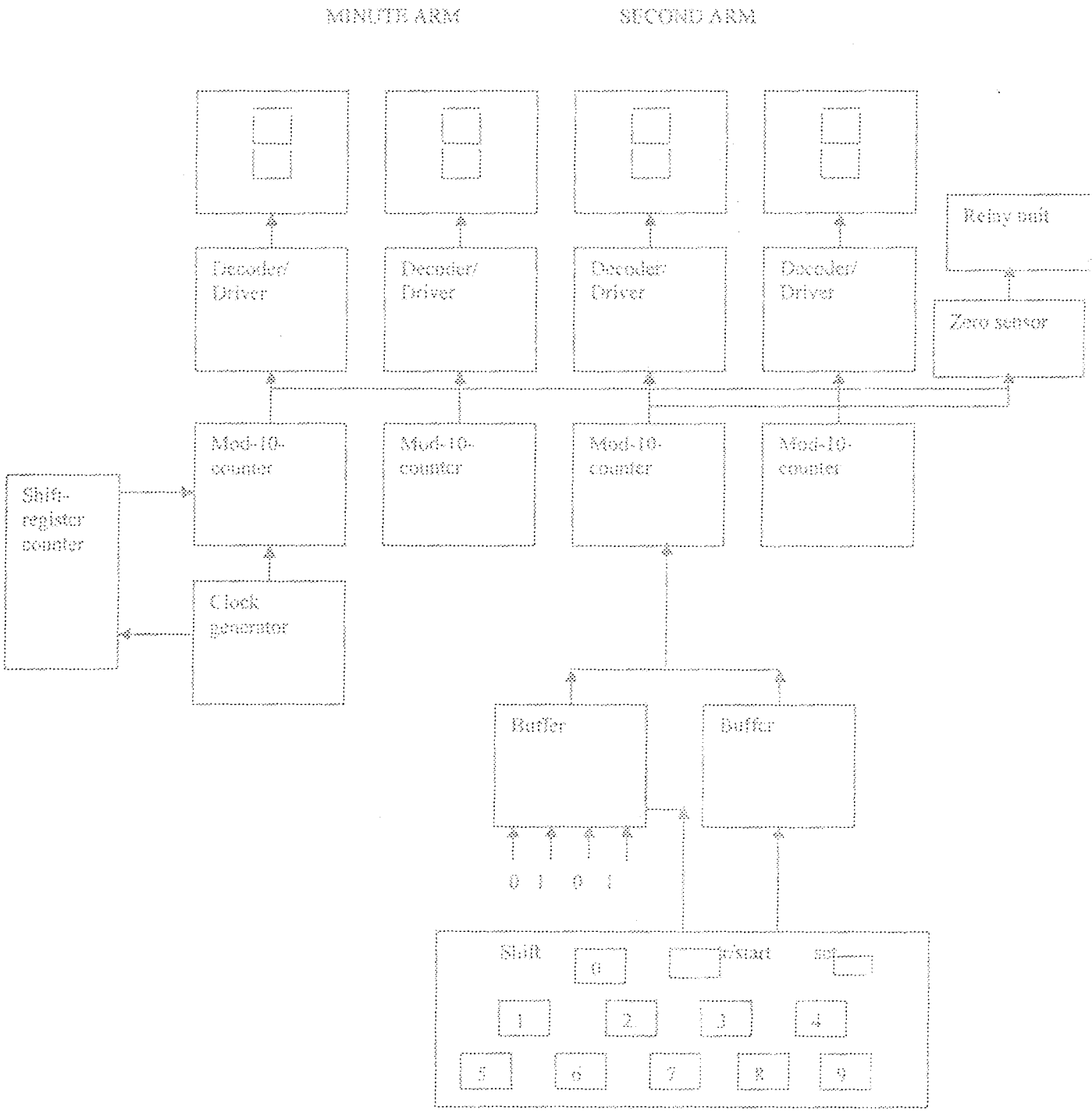


FIGURE 2.0 BLOCK DIGRAM OF THE TIMER

2.2.0 LOGIC FAMILY SELECTION

There are so many different logic families produced by different manufacturers.

At present there are three main logic families in common use

1. Transistor-Transistor Logic (TTL)
2. Complementary metal-oxide semiconductor (CMOS)
3. Emitter-coupled Logic (ECL)

Others include

4 Resistor Transistor Logic (RTL)

5 Diode Transistor Logic (DTL)

6 Integration Injection Logic (IL)

Complementary metal-Oxide Semiconductor (CMOS) orTransistor-Transistor Logic (TTL) should be able to satisfy most users' needs except where ultimate in speed is needed when emitter-couple logic should be chosen.

However, CMOS family is widely used and has very low power consumption and they are perfect for battery operated electronic devices, which satisfies the requirement for this project. Many large-scale integrated circuits (LSI) such as digital wrist watch and calculator chips are manufactured using the CMOS technology .The older 7400 series of TTL

logic devices has been extremely popular for many decades. But one of its disadvantages is its higher power consumption.

In late 1960s, manufacturers developed CMOS digital ICs and since then, many types of CMOS circuits are available and several families of compatible CMOS ICs have been developed. The first was 4000 series, the next comes 74C00 series so on. But for this project work 4000 series are used.

CMOS is the best choice for this project because of its low power consumption. The following reasons explains why CMOS are the best for this project.

a). They do not respond to very fast noise pulses or circuits glitches because of its slower speed.

b) They have large (good) noise immunity (rejection) than the other logic families.

c) It is possible to pack more gates into one ICs without running into heat dissipation problems because of lower power consumption.

d) They are readily available in the market.

e) They impose fewer restrains on the power supply (+3v to +18v at very low currents

2.3.0THE POWER SUPPLY UNIT (PSU)

The power supply unit forms an important aspect of the project construction. It is a very vital primary factor that determines whether the project works or not.

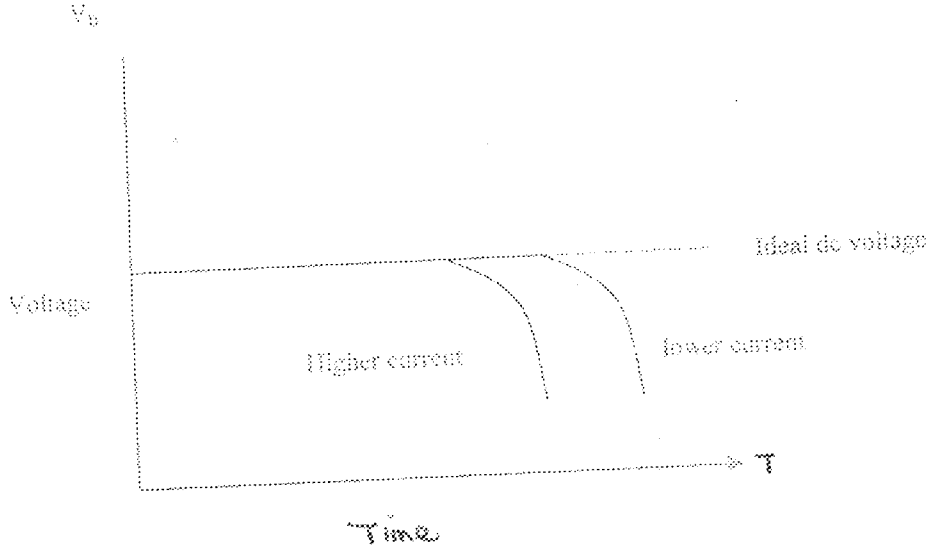
Generally, a battery usually drives CMOS and they use voltages ranging from (+3v to+18v). In this project 9v supplied from the battery is used to drive the circuit. Therefore, the difficulty of designing the power supply unit is extremely limited and also the use of power supply regulator IC is not required of the voltage range

The batteries convert the chemical energy of the constituents to electrical energy used to power the circuit.

FIGURE 2.1:THE CIRCUITS FOR A BATTERY.

The process of delivering power from the battery to the circuit can only last for a finite time. As current is drawn from the battery, the chemical components in the battery are consumed, the battery decreases towards zero and at this point the battery is discharged.

However, the rate of discharge of the battery depends on how much current that is drowned by the circuit. The battery lifetime is shorter at higher currents.



FIGGURE 2.2 THE BATTERY DISCHARGE CURVE FOR TWO DIFFERENT CURRENTS

2.4.0 THE CLOCK PULSE GENERATOR

2.4.1 THE QUARTZ CRYSTAL

Quartz crystal is the clock pulse generator used in this project .The quartz crystal has a mechanical resonant frequency at which it oscillates when it is excited. The operating frequency of the crystal used in this project is 32.768kh; that is 2^15 per second. Although a piece of quartz crystal can be cut to a specific shape and size tovibrate (resonate) at a precise frequency that is extremely stable with temperature and aging; frequencies from 10kh to80kh are readily achievable

The clock pulse from the output of the clock generator is fed into the counters, which count pulses from maximum pre-set count to zero.

Timers need to have accurate and stable clock pulses available thus, quartz crystal together with a simple circuit to generate digital pulses, fits this project need perfectly.

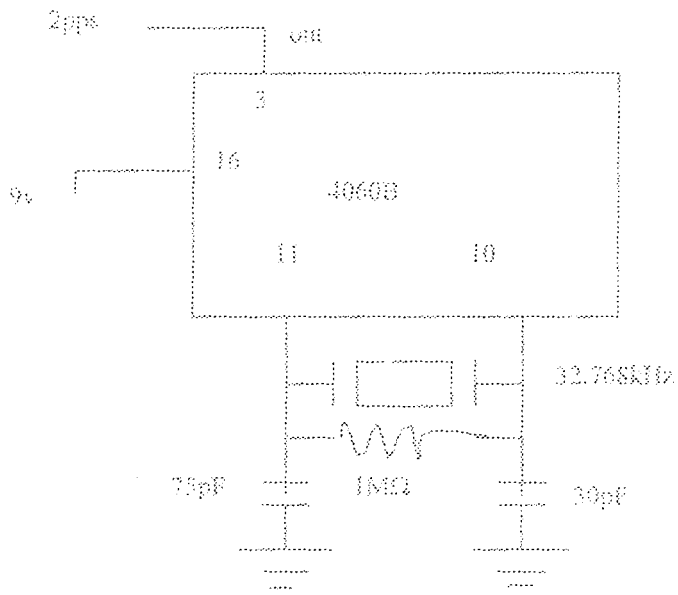


FIGURE 3.3:A CRYSTAL CONTROLLED DIGITAL OSCILLATOR CIRCUIT

2.4.2 CLOCK FREQUENCY DIVIDER/COUNTER

The frequency (32768hz) of the quartz crystal can not be input to the counters directly since they only require one pulse per second hence; frequency

divider/ counter/oscillator (4060B) is used to divide the frequency. It contains 14 flip-flops each divides the frequency of its input by 2 giving a clock pulse at 2pulse per second which is again divided by a J-K flip-flop connected to the divider to give 1pps required. The output of each flip-flop is a square wave fed into the counters.

2.5.0: SEVEN- SEGMENT DISPLAY AND DECODER/DRIVERS

2.5.1:SEVEN SEGMENT DISPLAY UNIT

The display arrangement used in this work use Light-emitting diodes (LED) for each segment .The LED display used is a common- cathode type where the cathodes of all the segments are tied together and connected to the ground. The display readout is driven by aBCD-7-segment decoder/driver with active high outputs that apply a HIGH voltage to the anode of that segment to be activated.

The i/p of the seven- segment display anodes are connected to the o/p of the CD4511Bdecoder.All the anodes of the LED's are connected to through current- limiting resistors to the appropriate outputs of the decoder/driver. By controlling current through each LED some segments will light (1) and others will be dark (0) so that the desired character pattern will be generated .For

example to display a "5", the segments a, f, g, c, and d are made HIGH (1) while segments b, and e are LOW (0).

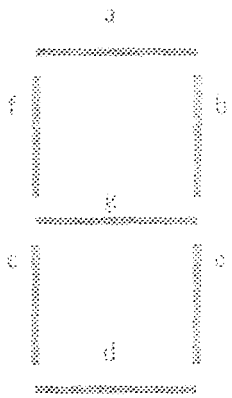


FIGURE 2.5 SEVEN-SEGMENT LED INDICATOR ARRANGMENT

The clock pulse counted by the Down counter is clearly readout from this segment unit. The LED's are chosen for this project because they have much brighter display than LCD's (liquid -crystal displays). They are easily visible in dark or poorly areas.

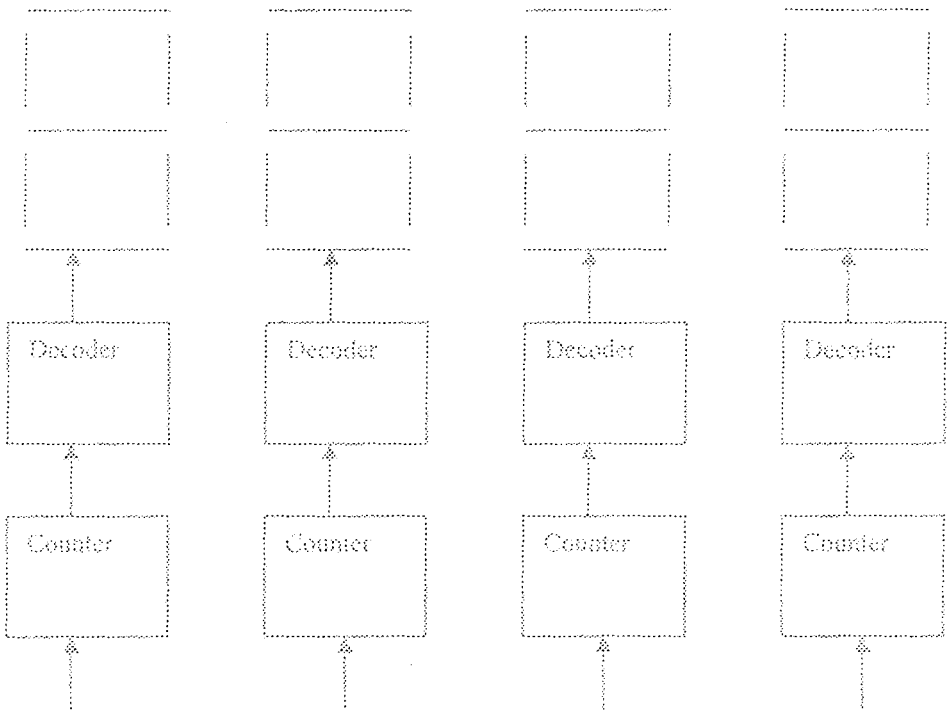
2.5.2 BCD-TO-SEVEN SEGMENT DECODER/DRIVERS

The BCD-to7-segment decoder driver is used to take a four –bit BCD input from the output of CD4029B IC counters and provide the outputs that pass current through the appropriate segment to display to display the decimal digits.

The decoder inputs that come from the output of the counter is being pulsed continually and the decoder/drivers output is activated sequentially

which is been used as timing signals acting through CD4078B IC NOR- gate (senses 0000signal at count down) to turn devices on or off at a specific time via relay.

FIGURE2.5: DECODER/DRIVERS AND SEVEN-SEGMENT MODULES CONNECTION



2.6.0 THE CONTROL UNIT

The control unit is the "heart" control part of the timer. It determines how the timer functions effectively. The major function is to preset the counters to the desired staring count or resetting the counters.

This unit consists of the Switches, Binary logic gates, and S-R flip-flop. They are all used for effective control operation of the timer.

2.6.1 BINARY LOGIC GATES

Binary logic gates are used in the construction of this project work to operate on a number of binary signals. The electronic gates packed in integrated circuits are used to operate on a number of binary signals to perform some logic functions.

Among the gates used include NAND gates, NORgates, INVERTERS (NOT) gates, OR gates, AND GATES.

The gates are discussed below.,

1) AND GATES

This is a circuit with two or more inputs and a single output. Its output is true if the two inputs are high.

2) OR GATES

It is a circuit with two or more inputs and a single output. The output is true when either or both of the its inputs are high.

3) NOT GATES

The inverter has only one input and one output. If the input is HIGH the output will be LOW.

4) NOR GATES

This is a combination of both OR and NOT gates.

5) NAND GATES

This gate is form using both AND and NOT gates.

2.6.2 THE SWITCHES

All the switches used in this design work are built on a panel ((pad) from which the operation of the timer is carried out using appropriate button to perfonm the desired operation.

The panel is a matrix of switches arranged in column and rows, depressing a switch short circuit a row and a column. The panel is connecied to the counters. Each switch has its peculiar function

2.6.3THE S-R LATCH

The CD4027B flip-flop integrated circuit has provisions for J, K, SET, RESET, and clock input signals. Therefore, inorder to use this J-K master flip-flop as S-R latch the clock, J, and K inputs are grounded. The SET and RESET

functions are independent of the clock and are initiated when a high level signal is present at either the set and reset input and the output signals are provided as buffered Q and Q.

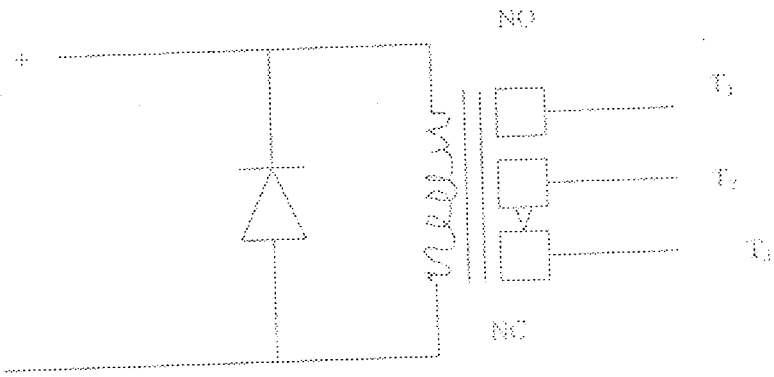
2.7 THE RELAY UNIT

The relay unit consists of the relay and the transistors, which are used to switch off the equipment.

The relay used is an electromagnetic relay, it consist of an electromagnet and a set of switch contacts which are normally closed or normally opened .A normally closed is the one which is closed when the relay is de-energized while a normally opened contact is one which is open when the relay is de-energized. Thus when the relay is energized, its contact change state

The transistors form a complementary switch hence when the transistors are turn 'ON', the relay is de-energized and when the transistors are 'OFF', the relay is energized.

FIGURE2.6: THE CIRCUIT DIAGRAM OF THE RELAY



When the transistors are saturated upon receiving signal from the logic level, it get saturated and then switch off the relay which in turn isolates the equipment from external high voltage (a.c) that power the equipment.

2.8 BUFFER

The buffer used is a HEX. Non-inverting 3-state buffer used for bus-orientated application in this work. It is used as an intermediate component between the counter and the panel which contains switches to prevent undesirable signal from been JAMED into the counter.

A high level on either disable input will cause those gates on its control inputs to go a HIGH impedance (i.e. very high resistance so that very small current flow through it) while a low level on either disable input will cause those gates on its control line to go a low impedance.

CHAPTER THREE

3.0 DESGN AND CONSTRUCTION OF THE COUNTER.

3.1 CLASSIFICATION OF COUNTERS

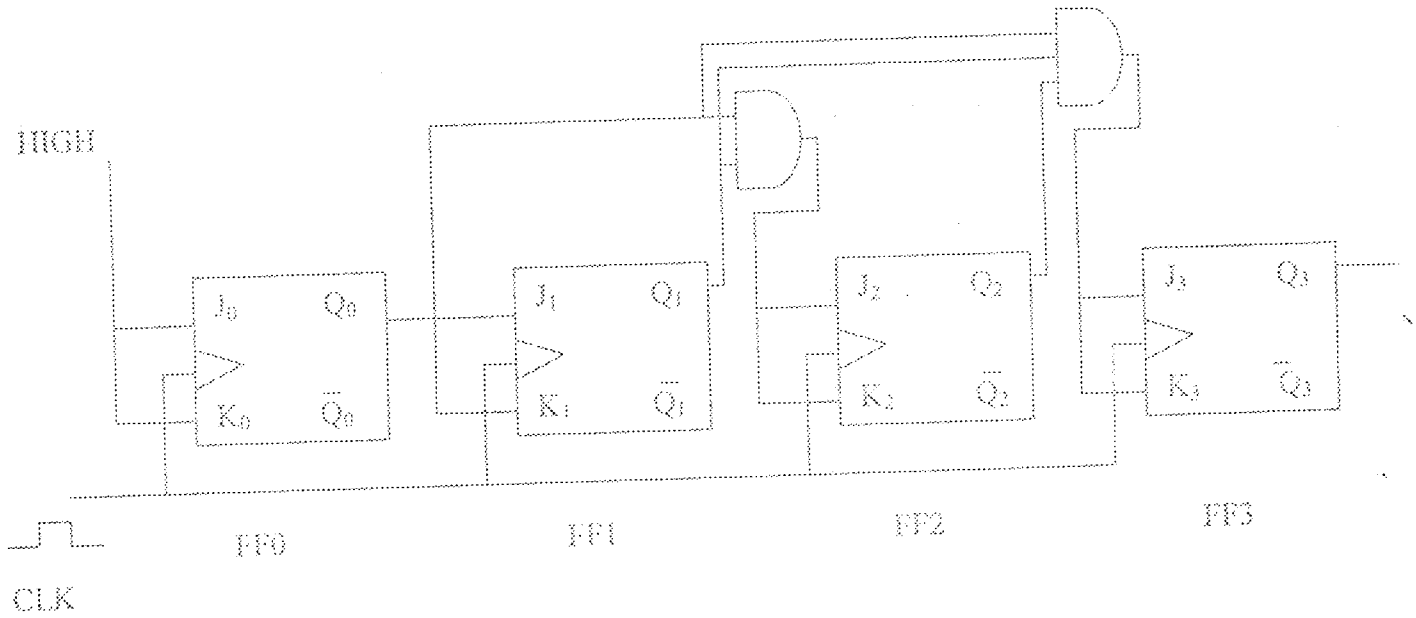
Counters are classified in to two broad categories according to the way they are clocked asynchronous and synchronous. In asynchronous counters commonly called RIPPLE COUNTERS, the external clock pulse clocks the first flip-flop and then each successive flip-flop is clocked by output of the proceeding flip-flop. In the case of synchronous counters which are used in this project, the clock input is connected to all of the flip-flop so that they area clocked simultaneously.

3.2.0: SYNCHRONOUS COUNTERS.

A synchronous counter is one in which all the outputs charge at the same time because all the flip-flops are directly clocked at the same tie by the input clock.

When the J and K inputs are low on a JK flop-flop, the output does not charge when the flip-flop is clocked; and if J and K are high, the flip-flop toggles when it is clocked.

FIG3.0 CURCUIT DIAGRAM OF A FOUR BIT SYNCHRONOUS COUNTER



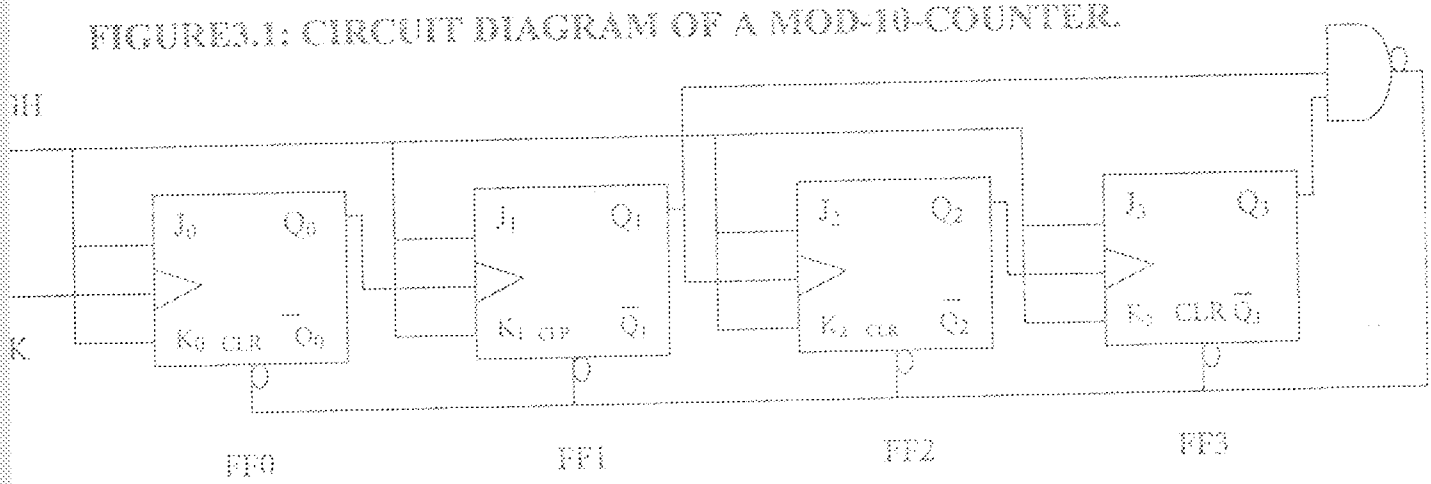
In other words, each flip-flop should have its J and K inputs connected such that they are HIGH only when the outputs of all lower-order flop-flops are in the HIGH state. The synchronous counters are otherwise known as PARALLEL COUNTERS.

3.3.0: SYNCHRONOUS DECADE COUNTER (MOD-10-COUNTERS).

The counters used in this work are synchronous MOD-10-counters. Counters could also be designed to have a number of states in their sequence that is less than the maximum of 2^n. the resulting sequence is called a TRUNCATED SEQUENCE. To obtain a truncated sequence, it is necessary

to force the counter to recycle before going through all of its normal states. For example, the BCD decoder counter must recycle back to the 0000 state after count of nine (1001) is to decode count ten (1010) with NAND gate and connect the output of the NAND gate to the clear (CLR) inputs of the flip-flops.

FIGURE3.1: CIRCUIT DIAGRAM OF A MOD-10-COUNTER.



A decade counter requires four flip-flops (three flip-flops are insufficient because $2^3=8$ i.e. 2^n). This type of counter is useful in display applications as used in this project work in which BCD is required for conversion to a decimal readout.

3.3.1 SYNCHRONOUS MOD-10 DOWN COUNTERS.

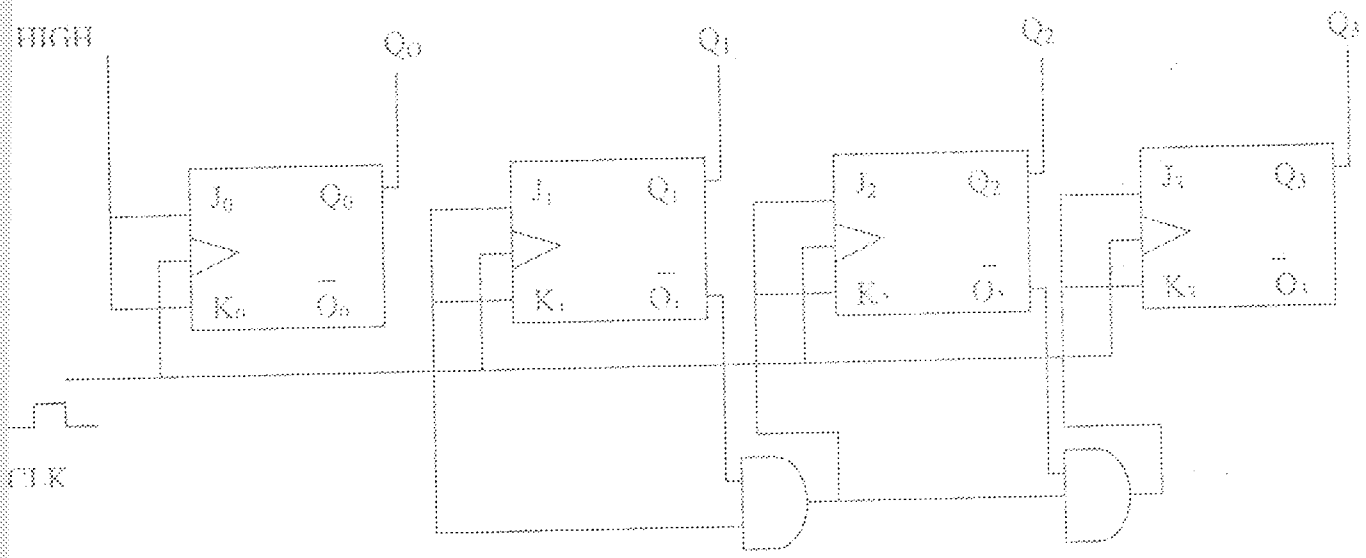
The synchronous (parallel) DOWN counters used in this work counts down form a maximum starting count to zero. Just as in counters each flip-flop toggles when clocked if J and K are HIGH.

The CD4029B counter used consists of a four-stage binary or BCD-decade up/down counter. A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock.

Binary counting is accomplished when the BINARY/DECADEE input is high. The parallel down counters are made to count down by using the inverted output of each flip-flop to drive the following J, K inputs.

This DOWN COUNTERS are normally used in situations where the desired number of input pulses that have occurred must be known, as is the desired in this project.

FIGURE3.2: CIRCUIT DIAGRAM OF A JK MOD-10 DOWN COUNTERS.



3.4 FLIP-FLOPS

Flip-flops (FFs) are synchronous bistable devices. The term synchronism means that the output changes state only at specified point on a triggering input called clock (CLK), i.e. changes in the output occur in synchronism with the clock.

An edge-triggered flip-flop changes state either at the positive edge (rising edge) or at the negative edge(falling edge) of the clock pulse and is sensitive to its input only at this transition.

The CD 4027B IC used is a dual J-K master flip-flop, the flip-flop is used to perform toggle function.

The logic levels present at the J and K inputs changes state in synchronism with the positive going transition of the clock pulse. On each successive chock spike, the flip-flop changes to the opposite state, this mode is called TOGGLE operation

TABLE 1: POSITIVE EDGE-TRIGGERED 4027 TRUTH TABLE

INPUTS					OUTPUTS		COMMENTS
S	R	CK	J	K	Q	$\overline{Q}$	
L	L	↑	L	L	Q_0	$\overline{Q_0}$	NO CHANGE
L	L	↑	H	L	H	L	RESET
L	L	↑	L	H	L	H	SET
L	L	↑	H	H	$\overline{Q_0}$	Q_0	TOGGLE
L	H	X	X	X	0	1	
H	L	X	X	X	1	0	
H	H	X	X	X	H*	H*	

KEY:

↑ : Clock transition low to HIGH.

X: irrelevant ("don't care")

Q_0 = Output level prior to clock transition.

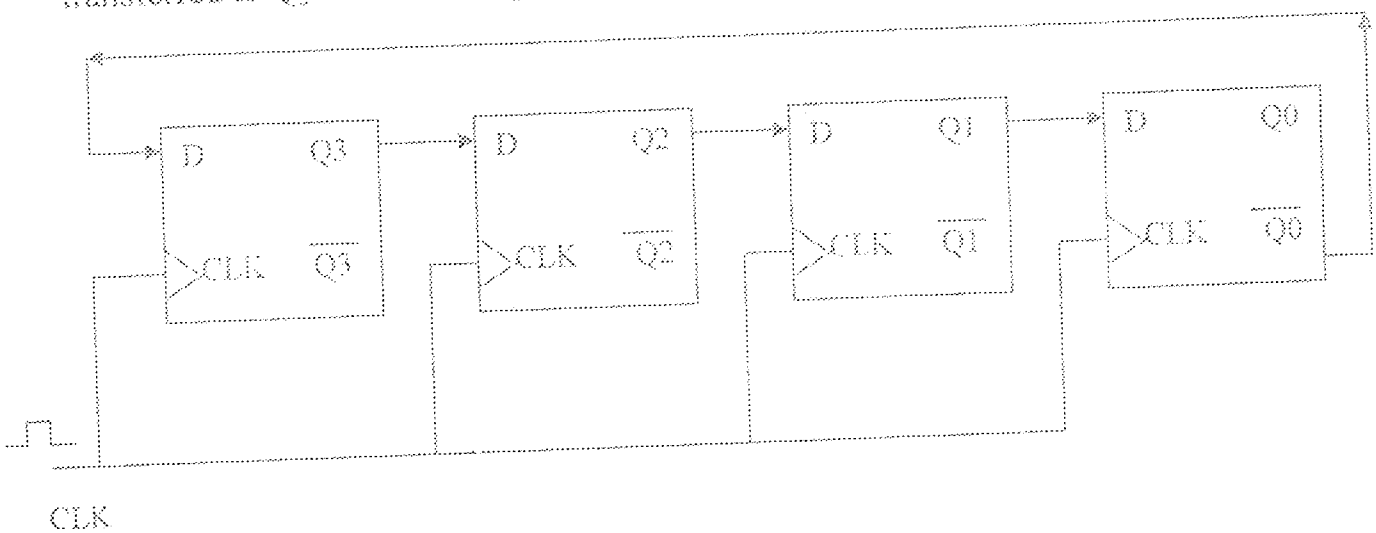
3.5 SHIFT- RECUSTER COUNTER

A shift – register counter is used to shift the date or value of flip- flop from left to right shift register counter has the output of the last flip-flop in the connected back to the first flip-flop.

JOHNSON COUNTER

A 4- stage divide- by -8 Johnson counter was used as Mod –8 counter, this mean it has eight distinct states before the sequence repeats. Although this circuit does not progress through the normal binary counting sequence it is still a counter because each count cones pond to a unique set of flip-flop states.

The design of Johnson or divested-ring counter is such that the inverted output of the last flip-flop is counted to the input of the first flip-flop. On each positive clock pulse transition, the Q_0. Output is connected back to the D input of Q_3. This mean that the inverse of the level stored in Q_3 will be transferred to Q_3 on the clock pulse,Q_2 in to Q_1 and Q_1 into Qo randomly.



FIUGURE 3.7: THE CIRCUIT DIAGRAM OF AMOD-8-JOHNSON COUNTER

TABLE 2: MOD-8-JOHNSON SEQUENCE TABLE

Q_3	Q_2	Q_1	Q_0	CLOCK PULSE
0	0	0	0	0
1	0	0	0	1
1	1	0	0	2
1	1	1	0	3
1	1	1	1	4
0	1	1	1	5
0	0	1	1	6
0	0	0	1	7
1	0	0	0	8
1	1	0	0	9

CHAPTER FOUR

4.1 DISCUSSION OF RESULTS

It was expected that when the clock generator is excited should generate clock-pulses using 'quartz crystal' having operating frequency of 32.768kh and this was achieved.

The Down counter which was obtain in the form of IC to minimize cost of building from discrete components, also function normally as expected producing counts from 9999 to 0000 the decoder and was display on the seven segment display unit

The relay was expected to switch the equipment at the end of maximum count to 0000 by the timer and this was successful.

The result of this project therefore was very satisfactory at testing. In other words design, research, and construction are successful.

4.2 THE CONSTRUCTION COMPONENTS

The construction of the timer was successful though with little limitations. Most of the components used were inform of IC, the availability of the equivalence in the components made the design and construction easier.

All the IC used belongs to the complimentary metal-oxide semiconductor family. The detailed lists of the components used are made below.

SERIAL NUMBER	COMPONENT TYPE	QUALITY
1	CD4511B Decoders	4
2	CD4029B Counters	4
3	CD4073B Tri - 3 - input AND gate	1
4	CD4060B Divider / Oscillator	1
5	CD4081B Quad 2 – Input AND gate	1
6	CD4011B Quad 2 – Input NAND gate	1
7	CD4022B Shift-register counter	2
8	CD4503B Buffer	2
9	CD4027B Dual – J-K master Flip Flop	2
10	CD4078B 8 – Input NOR gate	2

11	CD4069B Hex Inverter (NOT gate)	2
12	6V Relay	1
13	Transistors: 2SC403, 2SC945	1, 1
14	Resistors: 1kΩ, 33kΩ, 2.2kΩ, 1MΩ, 100Ω	1, 4, 1, 1, 4
15	Diode IN4181 IN4001	20 1
16	Bush buttons	12
17	Quartz Crystal	1
18	Capacitors: Ceramic, 75pf, 30of	1, 1
19	Soldering lead	Few yards
20	Seven segment LED indicator	4
21	Vero board	
22	Connection wires	Numerous
23	CD4071 Quad 2 – input or gate	2

CHAPTER FIVE

CONCLUSION

The design, construction of the programmable timer actually was not done hitch free. The availability of some components was not easy. But once they were obtained the work seem to be done. The testing of the prototype confirms the aim of the project. I do believe that this project work will meet the acknowledgment and approval of the industrial sectors where it is applicable.

RECOMMENDATIONS

Though the aim of this project work has been a complete successful one, it was achieved with some difficulties.

Problems were encounter in the area of attempting to use the rectified 9v d.c to power the circuit, instead of the normal common batteries used to operate CMOS hence further attempts should be made to use a.c rectified to power CMOS.

The department should make definite effort to improve on the type of practical carried out in the laboratory in electronics to expose the students early enough to similar projects to be embarked upon in their final year projects.