Design and Construction of a Digital Quiz Decider and Timer Device

By

Denga, Solomon Washima

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Dedication

This work is dedicated to the almighty God for his infinite mercies over me, and to my beloved mother Mrs. Comfort V. Denga.

Declaration

I, Denga Solomon Washima, declare that this work was done by me and has never been presented elsewhere for an award of a degree. I also hereby relinquish the copyright to the Federal University of Technology, Minna.

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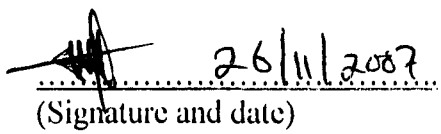
(Name of student)



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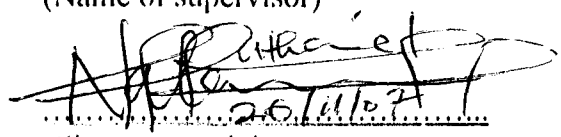
Mr. N. Salawu.....
(Name of supervisor)



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Engr. M.D Abdullahi.....
(Name of H.O.D)

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Acknowledgement

My profound gratitude goes to Jehovah God almighty, the one whom his infinite mercies has brought me this far.

My deep appreciation goes to my supervisor, Mr. N. Salawu for all his kindness, advice and understanding. I am glad to have tap from his wealth of experience.

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Finally, I recognized the contributions of my classmates and friends who assisted me in one way or the order in the course of this work.

Abstract

The digital quiz decider and timer device is a system designed to single out and time the contestant that indicate to answer a question being asked in a quiz contest or a game show. It therefore handles the function of a time keeper as well as increases the level of fairness to all contestants in a quiz contest. This is carried out automatically by the device without external interference.

The device therefore gives contestants equal opportunities and also reduces the amount of labor required to organize a quiz contest. The best out of the contestants are therefore known. Hence, the goal of organizing a quiz contest is achieved with this device.

The design is done using medium scale integration (MSI) integrated circuits (ICs) and discrete components like resistors and capacitors and could be divided into the following functional modules: the power supply unit, the selection and display unit and the alarm unit.

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Chapter One

1.1 Introduction

A competition in which people try to answer questions to test their knowledge is known as quiz. It is an informal test given to students or used in a game play. It comes in different forms depending on how the organizers want it. The competitors could be in groups or individually. In any case, either the contestants could pick questions at random or questions being asked generally for the first to answer correctly within a specified time. The focus in this project is that for individual contestants with questions being asked generally for the first to answer correctly.

The coordinators of a quiz contest include a quiz master who reads the questions in the competition, the recorder who records the scores for the contestants and the time keeper who monitors the time allowed for a question. The quiz master is also responsible for choosing any contestant who indicates by show of hand that he/she is ready to answer the question. He/she is therefore faced with the challenge of knowing who indicated to answer the question first.

Owing to the fact that a quiz contest plays an important role in encouraging students at the primary and post primary school levels as well as in games show, it became necessary to device a means of increasing fairness and efficiency in the process.

The digital quiz decider and timer device is designed to enable contestants in a quiz competition to answer a question as soon as they indicate their readiness to do so by pressing a switch assigned to them. The design is for a maximum of eight (8) contestants with the

number of the contestant that buzzed in first being displayed and an alarm sound indicating that a contestant is ready to attempt the question. Any contestant that buzzed in after the first contestant will not activate the circuit hence, eliminating the difficulty in identifying the contestant that signaled to attempt the question if it were by show of hands.

There is a RESET button to be assigned to the quizmaster to RESET the device after reading the question. This will ensure that, no contestant buzzed in before it was time for them to do so. [5]. There is a preset time of 16 seconds for a question also imbedded in the device with an alarm indicating when the time elapses. Thus, the role of a time keeper who may not be fair to all contestants is eliminated.

1.2 Methodology

Almost all of the digital circuits used in modern digital systems are integrated circuits (ICs). The wide range of available logic ICs has made it possible to construct complex digital systems that are smaller and more reliable than their discrete-components counterparts.

Several integrated circuits fabrication technologies are used to produce digital ICs, the most common being TTL, CMOS, NMOS, and ECL. Each differs in the type of circuitry used to provide the desired logic operation. For example, TTL (transistor transistor logic) uses the bipolar transistor as its main circuit element, while CMOS (complementary metal-oxide semiconductor) uses the enhancement-mode MOSFET as its principal circuit element. A family of TTL circuits is available under manufactures numbers starting with the designation 74. These families of TTL circuits provide various logical and functional characteristics with well specified speed, power dissipation, etc features. Of the various types

of the 74 series of TTL circuits, the LS series is the most popular, providing fast speed and low power dissipation. [3].

In digital electronics, there are only two logic states present at any point within a circuit. These voltage states are either HIGH or LOW. The meaning of a voltage being HIGH or LOW at a particular location within a circuit can signify a number of things. It may represent that one bit of a number, or whether an event has occurred, or whether some actions should be taken. The high or low states can be represented as true or false statements which are used in Boolean logic. It is therefore logical to use binary numbering system to keep track of information.

A binary number is composed of two digits, 0 and 1 also called bits (e.g. 0=low voltage while 1=high voltage). It is the most important numbering system in digital systems, but several others are also important. The decimal system is important because it is universally used to represent quantities outside a digital system. This means that there will be situations where decimal values must be converted to binary values before entering them in to the digital system and vice versa.

In addition to binary and decimal, two other number systems find widespread applications in digital systems. The octal (base 8) and hexadecimal (base 16) number systems are both used for the same purpose to provide an efficient means for representing large binary numbers. Both of these number systems have the advantage that they can be easily converted to and from binary.

In this project, the four number systems above are in use at the same time for design and construction of the digital quiz decider and timer circuit. The IC chips used to achieve this aim though were not found in Minna, they were however found in Oshodi Market in Lagos.

1.3 Aims and Objectives

The design and construction of digital quiz decider and timer devise is aimed at achieving the following aims;

i. It introduces the student to the practical application of the theory of courses taught in the classroom. Such courses as Analogue, Digital and Power electronics etc.

ii. The device produced is aimed at increasing the transparency, fairness and general efficiency in quiz competitions so as to know the best out of the contestants.

iii. A further look at the device indicates that it reduces the amount of labor required to organize a quiz contest.

A situation where the time lag between two contestants that buzzed in is in nano seconds, it becomes difficult to determine the fairness of the device.

Chapter Two

2.1 Literature Review

The increasing need and demand for a precision circuit, which could serve as a quiz circuit has been over the years. The much needed circuit upon design should be able to meet the basic requirement for the conditions found in a quiz contest or show. It should make possible at least for a situation where a person could be singled out among a group of players in a game show or contestants in a quiz contest as the first person who knows the question or who wants to make a trial first before others.

Talking advantage of the advancement in technology that has brought about availability of integrated circuit in their compact form as well as other passive and active components, electronics circuit designers took up the challenge of designing a circuit that could perform the aforementioned function.

Mr. Ane made an effort in year 2003 at designing a 4-input circuit that could serve in part the above mentioned purpose, employing the use of CMOS ICs and light emitting diodes (LEDs). Whereas this circuit will be able to select a desired person out of four contestants, it did not produce an audio visual alert to that effect. Hence, it was not a very effective device for the desired purpose. [9].

Another designer made an improved effort at designing one that could serve for eight contestants and at the same time produce an audiovisual alert as well as time out indication. He made use of semiconductor rectifiers (SCRs). However, his display was a

light effect by light emitting diodes with different colors for each contestant. [5]. All these left an opportunity for a research in to designing a circuit which would give a display of the actual number assigned to the contestant who indicates to answer the question first (decimal display) and at the same time sound an alert indicating that somebody has been chosen. This alarm last for 1 second indicating the beginning of the time for a question. When the time for a question elapses, the alarm sound for the second time indicating the end of the time allocated for a question. This can be achieved using 555 timer/oscillators.

2.2 Digital IC Technology

Digital IC technology has advanced rapidly from small scale integration (SSI), with fewer than 12 logic gates per chip; through medium scale integration (MSI), with 12 to 99 equivalent gates per chip; on to large-scale and very large-scale integration (LSI and VLSI), which can have tens of thousands of gates per chip, etc.

Most of the reasons that modern digital systems use integrated circuits are obvious. ICs pack a lot more circuitry in a small package, so that the overall size of almost any digital system is reduced. The cost is dramatically reduced because of the economies of mass-producing large volumes of similar large volumes of similar devices. Some of the other advantages are not so apparent.

ICs have made digital systems more reliable by reducing the number of external interconnections from one device to another. Before we had ICs, every circuit connection was from one discrete component (transistor, diode, resistor, etc) to another. Now, most

of the connections are internal to the to the ICs, where they are protected from poor soldering, breaks or shorts in connecting paths on a circuit board, and other physical problems. ICs also dramatically reduced the amount of electrical power needed to perform a given function, since their miniature circuitry typically requires less power than their discrete counterparts. In additions to the savings in power-supply costs, this reduction in power has also meant that a system has a system does not require as much cooling.

Some of the limitations of some of these ICs include their inability to handle very large currents or voltages because the heat generated in such small spaces would cause temperatures to rise beyond acceptable limits. In addition, ICs can not easily implement certain electrical devices such as inductors, transformers and large capacitors. For these reasons, ICs are principally used to perform low-power circuits operations that are commonly called information processing. The operations that require high power level or devices that cannot be integrated are still handled by discrete components.

The various logic families differ in the major components used in their circuitry. e.g. transistor transistor logic (TTL) uses bipolar transistors as their major circuit element.

2.2.1 Encoders

An encoder is intended to operate with inputs which have the feature that at any time, one is singled out to have a logic level different from all the others. Digital systems

frequently include components intended to generate signals indicating that some action needs to be taken.

Priority encoders include the necessary logic to ensure that when two or more inputs are activated, the output code will correspond to the highest numbered input. The priority encoder IC chip 74147 functions as a decimal-to-BCD priority encoder. It has nine active-low inputs representing the decimal digits 1 through 9, and it produces the inverted BCD code corresponding to the highest-numbered activated input. The truth table for a nine input priority encoder is shown in table 2.1.

Table 2.1: Truth table for IC chip 74147 priority encoder.

$\overline{A_1}$	$\overline{A_2}$	$\overline{A_3}$	$\overline{A_4}$	$\overline{A_5}$	$\overline{A_6}$	$\overline{A_7}$	$\overline{A_8}$	$\overline{A_9}$	$\overline{Q_3}$	$\overline{Q_2}$	$\overline{Q_1}$	$\overline{Q_0}$
1	1	1	1	1	1	1	1	1	1	1	1	1
x	x	x	x	x	x	x	x	0	0	1	1	0
x	x	x	x	x	x	x	0	1	0	1	1	1
x	x	x	x	x	x	0	1	1	1	0	0	0
x	x	x	x	x	0	1	1	1	1	0	0	1
x	x	x	x	0	1	1	1	1	1	0	1	0
x	x	x	0	1	1	1	1	1	1	0	1	1
x	x	0	1	1	1	1	1	1	1	1	0	0
x	0	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0

The first line in table 2.1 above shows all inputs in their inactive HIGH state. For this condition the outputs are all 1111, which is the inverse of 0000, the BCD code for 0. The second line in the table indicates that a LOW at A9 regardless of the state of the other inputs will produce an output code of 0110, which is the inverse of 1001, the BCD code for 9. The third line shows that a LOW at A8 provided that A9 is HIGH, will produce an output code of 0111, the inverse of 1000, the BCD code for 8. In a similar manner, the remaining lines in the table show that a low at any input, provided that all higher numbered inputs are HIGH, will produce the inverse of the BCD code for that input [2].

2.2.2 7-Segment Display

Most digital equipments have some means of displaying information in a form that can readily be understood by the user or operator. This information is often numerical data but can also be alphanumeric. One of the simplest and most popular methods for displaying numeric digits uses a 7-segment configuration to form the decimal characters 0 through 9 and sometimes the HEX characters A through F. one common arrangement uses light emitting diodes (LEDs) for each segment. By controlling the current through each LED, some segments will be light and others will be dark so that the desired character pattern will be generated [3].

2.3 Difficulty That Limit Performance.

Since the device has to do with buzzing in through switches, there could be time lag especially in RESETING the device. The RESET switch is to be controlled by the quizmaster or the coordinator immediately after a question is read. This may lead to denial of the first contestant that would have buzzed in to do so hence, reducing the efficiency of the device.

Chapter Three

3.1 System Design and Analysis

The design of the Digital Quiz Decider/Timer device was approached with simplicity in mind. Modular design was therefore adopted with three modules as follows; the power supply unit, the selection/display unit and the alarm unit. The block diagram of the design is shown in fig3.1.

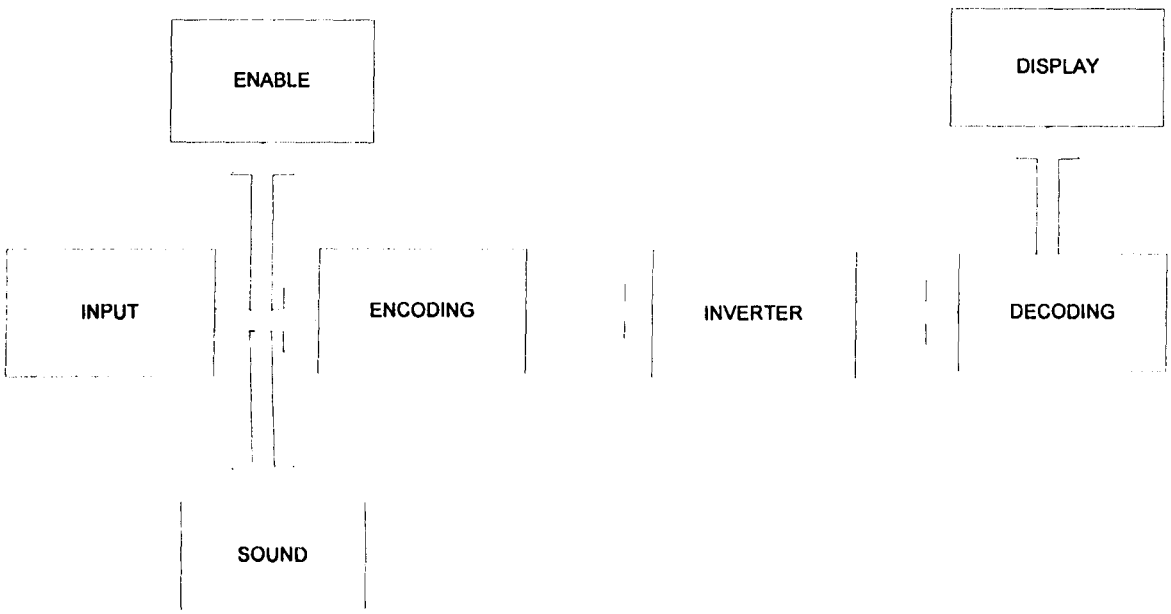

Fig 3.1: Block diagram of the design.

3.2 Power Supply Unit

All electronic devices require a direct current (dc) voltage source to operate. Very often, a circuit that converts the readily available alternating current (ac) supply to dc voltages is used. This system uses one of such circuits to provide the required voltages for operation. A block diagram of the power supply unit and the waveform at each stage is shown in fig 3.2.

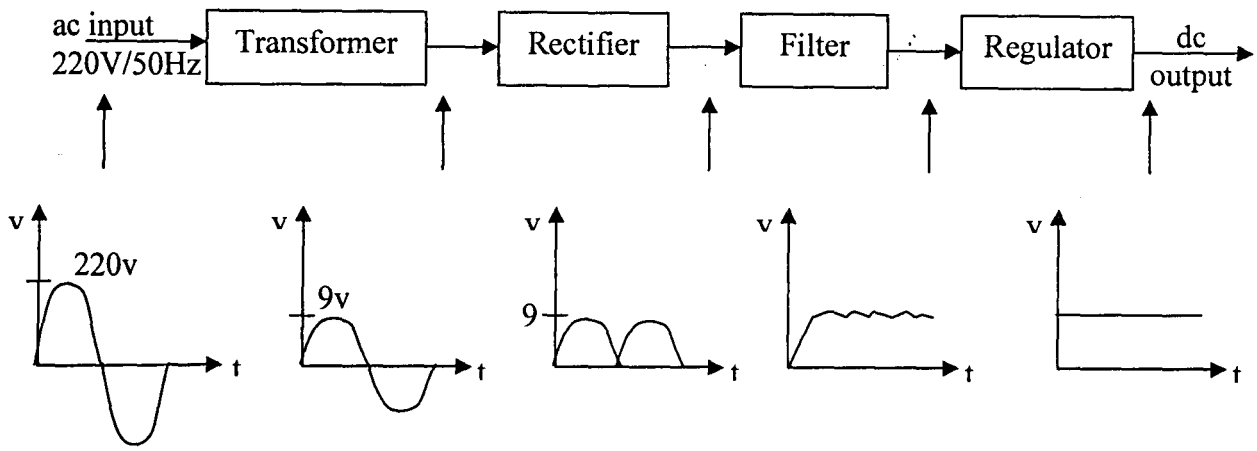

Fig. 3.2: Power supply block diagram and waveforms.

3.2.1 The Transformer

The first stage of the power supply design involves the stepping down of the 220V ac from the mains to about 12V ac with the aid of 220V/12V, 500mA transformer, whose current capacity is enough to drive the entire circuit.

The transformer is an electrical device that provides electrical isolation between the 220V ac mains and the rest of the circuit. The only link is by means of magnetic flux, thus eliminating the risk of shock. It consists of two coils, the primary (input) winding and secondary (output) winding. Figure 3.2 shows the circuit symbol of a transformer. The ratio of the primary voltage to that of the secondary V_2 is equal to the number of turns in pruning winding to that in the secondary winding n_2;

$$\frac{V_1}{V_2} = \frac{n_1}{n_2} \qquad \text{- - - - - - - - - - - - - - - (1)}$$

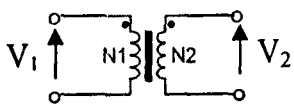

Fig. 3.3: Transformer.

A fuse (3A) is incorporated at the primary side to protect the transformer and the rest of the circuit from excessive current from the mains.

3.2.2 The Rectifier

The rectifier converts the 12V ac voltage from the transformer into a pulsating dc voltage and the process is called rectification.

A full-wave bridge rectifier is used for the rectification, it consist of four IN4001 diodes in the arrangement shown in figure 3.3 below.

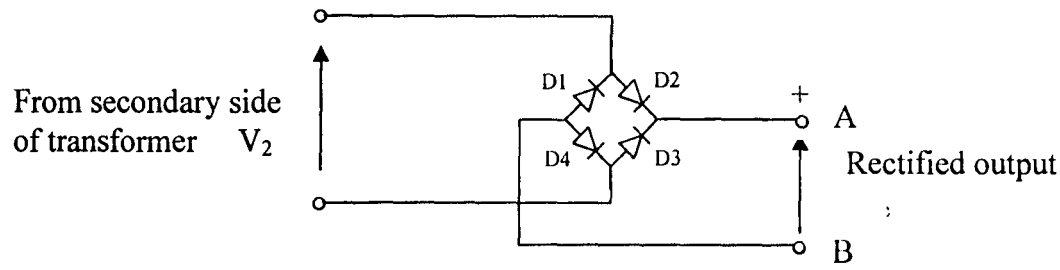

Fig. 3.4: Full-wave bridge rectifier.

During the positive half cycles diodes D2 and D3 are forward biased and current flows through any load connected at terminals AB. in the negative half cycle, diodes D1 and D4 are forward biased. Since the load current is in the same direction in both half cycles, the full-wave rectified signal appears across the load. The average dc voltage Vdc across AB is:

$$V_{DC} = \frac{2V_{2(peak)}}{\pi} = \frac{2\sqrt{2}V_{rms}}{\pi} = \frac{2\times\sqrt{2}\times 12}{\pi} = 10.80V$$

Where $V_{2\,(peak)}$ and V_{rms} are the peak output and the root mean square voltages of the secondary winding of the transformer respectively.

The diodes were so chosen such that their peak inverse voltage (PIV) rating is greater than $V_{2(peak)}$, so that they do not break down when reverse biased.

3.2.3 The Filter

The pulsating dc voltage from the rectifier is only suitable for limited applications such as charging batteries and running dc motors. Most electronic circuits require dc voltage that is constant in value. A filter is used to convert the full-wave rectified signal into a constant dc voltage.

Capacitive filtering is adopted in this design where a large electrolytic capacitor is connected across the rectifier output. The capacitor charges up during the diode conduction period to the peak value, and when the rectifier voltage falls below this value, the capacitor discharges through the load, so that the load receives almost steady dc voltage. The discharge time constant, which is the time taken for the capacitor to drop to 33% of the peak value is given thus:

$\tau_d = R_L C$ ---------- (2).

Where R_L is load resistance, C is capacitance.

Since R_L is a constant for any given circuit, it follows that the larger the C, the smaller the ripple voltage. A 2200μF, 25V capacitor was chosen for this circuit, which is large enough for the intended purpose.

3.2.4 The Regulator

The output voltage of the filter capacitor varies when load current or the input voltage varies. This effect is also undesirable.

Two monolithic voltage regulator IC chips, 7809 and 7805 are used to supply steady 9V and 5V to drive the alarm unit and energize the rest of the circuit respectively. These regulator chips supply the rated voltage with a wide range of voltage input (7V to 35V) and

variations in the load current. Small capacitors (1μF) are connected at their outputs to filter off any ripples left on the supply line. Figure 3.4 is a complete circuit diagram of the power supply unit [8].

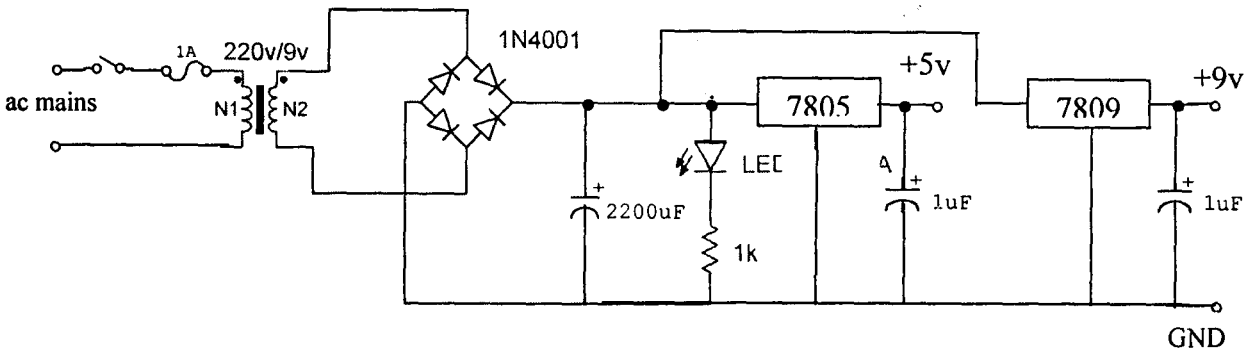

Fig. 3.5: Power supply unit circuit diagram.

3.3 Selection and Display Unit

The selection and display unit was designed with speed and accuracy in mind in achieving the desired goal.

3.3.1 Octal "D" Transparent Latch

An octal "D" transparent latch IC chip 74373 was used. It operates in an active LOW state and transfers whatever is at the INPUT pins to the OUTPUT pins. It also enables the design to accommodate up to eight (8) contestants since it has eight (8) INPUT pins. These INPUT pins are connected to eight (8) switches meant for the contestants and numbered accordingly on the switching panel.

The octal "D" transparent latch feeds a priority encoder from its output pins. It therefore solves the challenge of higher priority by the encoder. This was done using the enable pin of IC chip 74373 which automatically disables the IC after the first input hence

not taking any input until after RESET. This pin was connected to the RESET switch to be assigned to the quiz master.

Table 3.1: Truth table for IC chip 74373.

EN	$\overline{D_1}$	$\overline{D_2}$	$\overline{D_3}$	$\overline{D_4}$	$\overline{D_5}$	$\overline{D_6}$	$\overline{D_7}$	$\overline{D_8}$	RESET	$\overline{Q_8}$	$\overline{Q_7}$	$\overline{Q_6}$	$\overline{Q_5}$	$\overline{Q_4}$	$\overline{Q_3}$	$\overline{Q_2}$	$\overline{Q_1}$
x	x	x	x	x	x	x	x	x	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	0	1
1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1
1	1	1	1	0	1	1	1	1	0	1	1	1	1	0	1	1	1
1	1	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	0	1	1	0	1	1	1	1	1
1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1

From the above table we have that; when EN is HIGH, the D input will produce a low at the corresponding position and will latch to cause Q to become the same level as D. if D changes while EN is HIGH, Q will follow the changes exactly. To eliminate this, the connection is done such that as soon as the first D input is taken, EN goes LOW causing the Q outputs to remain at whatever level they had just before EN went LOW. That is, the outputs are "latched" to their current level and cannot change while EN is low even if D changes [8].

3.3.2 Priority Encoder IC chip 74147

This priority encoder functions as a decimal –to-BCD priority encoder. It is fed from the output of the octal "D" transparent latch. These active LOW inputs represent the decimal digits 1 through 9.

3.3.3 Hex Inverter IC chip 7404

The output from the priority encoder was inverted in to the normal BCD codes. This was achieved using the 7404 Hex inverter IC chip.

3.3.4 Seven Segment Display and Decoder

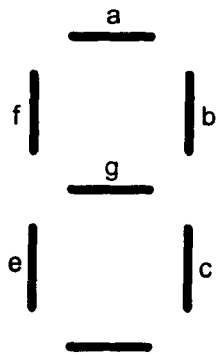

Fig. 3.6: A segment arrangement for a 7-segment LED.

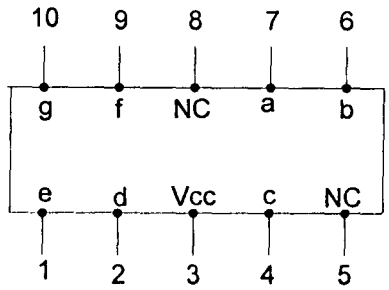

Fig. 3.7: Connection diagram for a 7-segment display.

The seven segment display used here is the common anode type where the anodes of all the LEDs are tied together in common and a single supply voltage is applied to this connection (Vcc). Since the decimal digits are presented in BCD form from hex inverter IC chip and we want to present the digits on a 7-segment display, we require a code converter. Hence, the incoming 4-bit BCD input will provide the outputs that will pass current through the appropriate output code word to illuminate the proper segments.

A BCD-to-7-segment decoder/driver is used to take a four-bit BCD input and provide the outputs that will pass current through the appropriate segments to display the decimal

digit. The decoder/driver has active-LOW outputs which are open collector driven transistors that can sink a fairly large current. This is because LED readouts may require 10 to 40mA per segment, depending on their type and size [3].

The resistor values are determined from the formula;

$$R_S = \frac{V_{CC}}{I} \Rightarrow I = \frac{V_{CC}}{R_S} = \frac{5}{360} = 0.0139$$
$$\Rightarrow I = 13.9mA$$

3.3.5 Information Flow in Fig 3.8

Initially on power on, all the inputs to IC1 are HIGH. All the eight outputs of IC1 are connected to inputs of priority encoder, IC2 as well as 8-inputs NAND gate, IC5. The output of IC5 thus becomes logic '1' which after inversion by NAND gate gives logic '0' at point 'x'. This output is again inverted by the NOT gate to feed pin 11 of IC1 making IC1 still active.

With all inputs to IC2 being high, its BCD output is 0000 after being inverted by IC3, which is applied to the seven segment decoder/driver, IC4. Thus on power on, the display shows '0'. This same process happens when the RESET switch is momentarily pressed and released.

When any of the push-to-on switches (S1through S8) is pressed the corresponding output line of IC1 is latched at logic '0' level and the display indicates the number associated with the specific switch. Since one of the inputs to IC2 is LOW (logic '0') giving an appropriate BCD output after being inverted by IC3which is applied to 7-segment decoder/driver hence, the display shows the number appropriately.

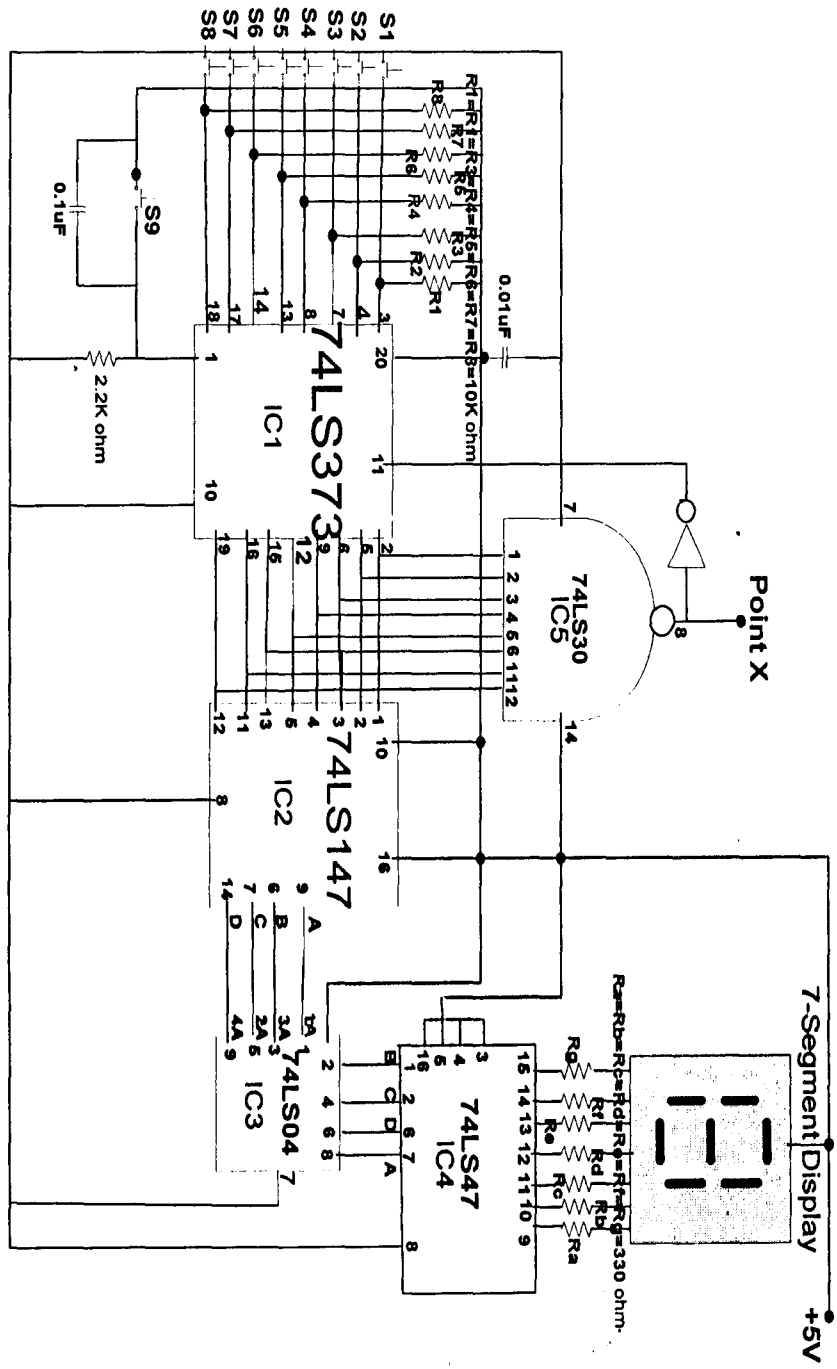

Fig. 3.8: Selection/display unit circuit diagram.

The IC1 output also serve as inputs to IC5giving rise to logic '1'at point 'x' this output is inverted using a NOT gate giving rise to logic '0'which inhibits IC1. Thus, pressing of any other switch S1 through S8 has no effect. This solves the challenge of higher priority in IC2.

Thus, the contestant who presses any of the switches S1 through S8 first jams the display to show only his number. In the unlikely event of simultaneously pressing two or more switches with the time lag of very few nana-seconds, the higher priority number will be displayed. However, this is unlikely to happen in practice. [3, 1].

3.4 The Alarm Circuit

The alarm circuit was designed with accuracy in mind. The circuit diagram is shown in fig 3.10. To make the 555 timer work, a trigger pulse at pin 2 initially sets the 555's internal flip-flop 'on'. It does so by comparing the input pulse to 1/3 of the supply power to a second comparator. This turns off the transistor across the timing capacitor and allows the timing capacitor to start the charge cycle. The 555 stays 'on' until this timing cycle turns it 'off' again by resetting the control flip-flop. The timing cycle can be made to start over again by applying a pulse to pin 4 (reset).this turns on the transistor that discharges the timing capacitor, and so delaying the charge from reaching 2/3 Vcc.

When the threshold at pin 2 drops, at the end of a timing cycle, the voltage drop can be used to start a new timing cycle right away by connecting pin 6 (threshold) to pin 2, the trigger input. This type of system is called "astable, free running oscillator" and was used in this design. Fig 3.9 shows the internal circuitry of the 555 timer IC chip [7].

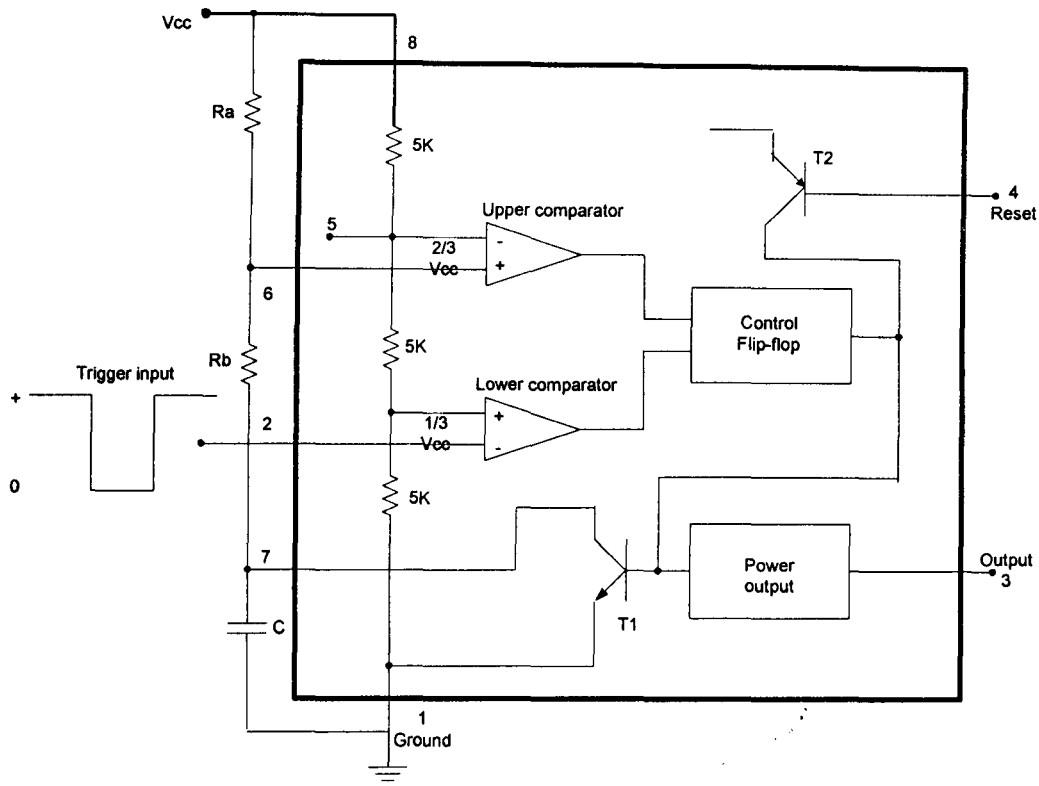

Fig. 3.9: 555 timer IC chip internal circuitry.

3.4.1 Design and Analysis of the Alarm Unit

The input to from point 'x' into the alarm circuit must be high (logic '1') to activate it. This implies that the alarm circuit will only come on when one of the inputs in to the S1 through S8 in fig 3.6 is pressed (goes low). From fig.3.10 R0 acts as a current limiting resistor for the optocoupler's LED. The current through the LED is given by the formula;

$$I_D = \frac{V_S - V_D}{R_0} \text{ ----(3)}$$

Where V_S = supply voltage to LED

V_D = voltage drop across LED

$\approx 1.2V$

And R_1 = current limiting resistor = $150\,\Omega$

$$\Rightarrow I_D = \frac{5-1.2}{150} = 0.0253A = 25.3\text{mA}$$

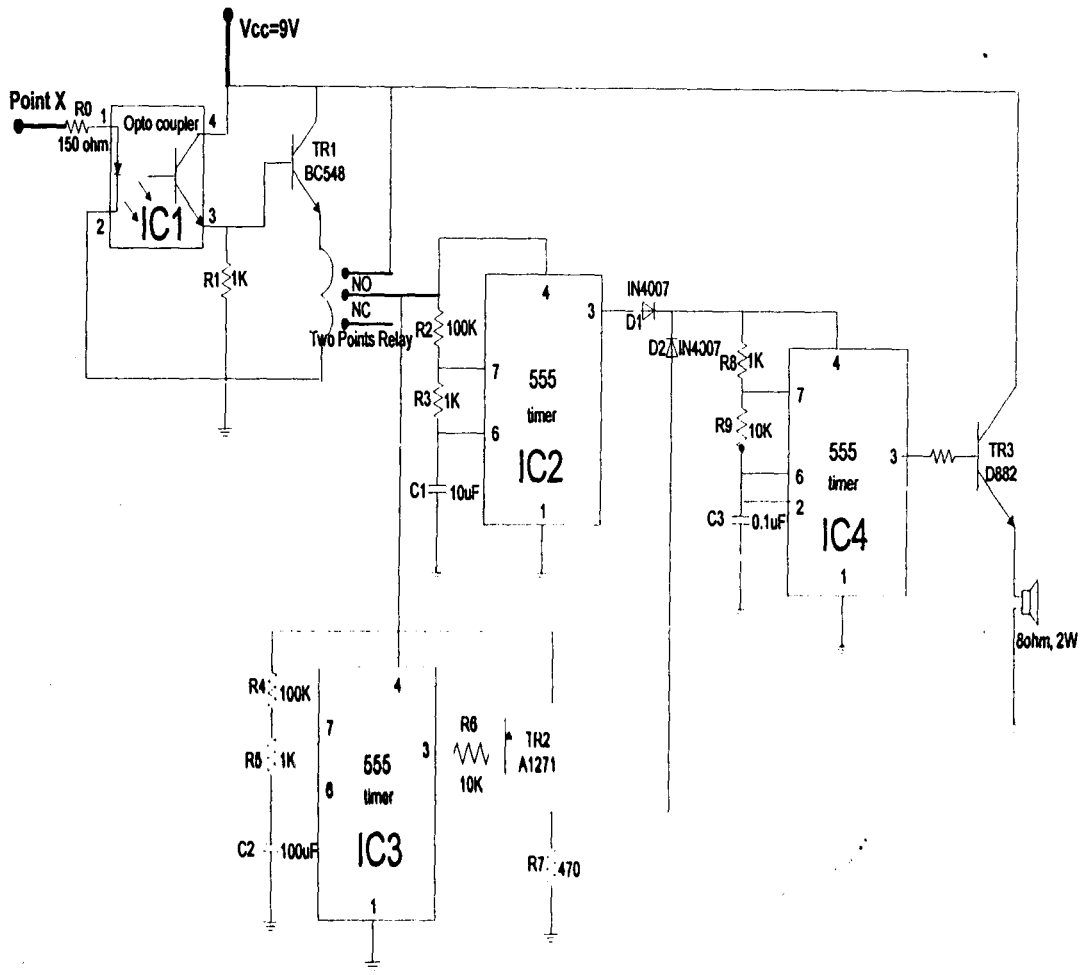

Fig. 3.10: The alarm circuits diagram.

The illumination from the LED caused by the current flowing through it drives the optocuplers photo transistor into saturation causing 9V drop across the emitter resistor R1. R1 biasing of TR1 (BC548) while the resistance of the relay coil acts as the load or emitter

resistor [6]. The relay is in a normally closed position with its coil having a resistance of about 200Ω. Since TR1 is operating as a switch, it must be driven into saturation mode.

Hence, we have;

$$Ic(sat) = \frac{Vcc}{Rc(sat)} \text{----------(4)}$$

$$\therefore Ic(sat) = \frac{9}{200} = 0.045A = 45mA$$

D.C current gain of the transistor, $\beta = hfe$ of the transistor = 200 typical (from the manufacturers).

$$\therefore I_B(sat) = \frac{I_C(sat)}{\beta} \text{-------(5)}$$

$$\Rightarrow I_B(sat) = \frac{45\times10^{-3}}{200} = 225uA$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} \text{--------(6)}$$

$$\Rightarrow R_B = \frac{5-0.6}{225\times10^{-6}} = 19555.6 = 19.6K\Omega$$

But for saturation to be guaranteed, the transistor was overdriven by a factor of 10 hence, Rb = 1955.6 = 1.96KΩ. The nearest available value for Rb = 2000 = 2KΩ.

IC1 is configured as a 1second monostable timer while IC2 is configured for 15seconds. The 1 second high output of IC1 supplies IC3 which is configured as a 800Hz frequency oscillator. Its output is further busted by transistor TR3 to drive the moving coil speaker for I second after which it goes off.

IC2 gives a high output for b16 seconds but this only reverse bias the PNP transistor and so, does not supply IC3 until after about 16 seconds when the output of IC2 goes low. This switches on the PNP transistor and IC3 begins to oscillate once again and the speaker

continues to wail until the RESET button in fig 3.6 is pressed to bring the output at point 'x' to low (logic 0). This will break the relay through the optocoupler. The diodes D1 and D2 prevent output from IC1 into IC2 and vice versa.

Timing period T, of the 555 timers is given by the formula;

$T = 1.1RC$ ---------- (7) Where R = $R_A + R_B$ ---------- (8)

For IC1 we have; R = 100K + 1K and period T, = 1second

$$C_1 = \frac{1}{1.1 \times 101000} = 9 \times 10^{-6} = 9uF$$

But the nearest standar-6d value is = 10uF

For IC2 we have; period T, = 15 seconds, $R_A = 100K\Omega$, $R_B = 1K\Omega$

$$\Rightarrow C_2 = \frac{16}{1.1 \times 10100} = 135 \times 10^{-6} = 135uF$$

But the nearest standard value is $= 100uF$

It is desired that the switching transistor TR2 sources 20mA for IC3 hence,

$$\therefore R_7 = \frac{V_{CC}}{I_{C(sat)}} = \frac{9}{20 \times 10^{-3}} = 450\Omega$$

But the nearest standard value $= 450\Omega$

$\beta = 200$ typical (from the manufacturer)

$$I_B = \frac{I_E}{\beta + 1} = \frac{20 \times 10^{-3}}{201} = 9.95 \times 10^{-5}$$

$$\therefore I_B = 99.5uA$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{9 - 0.6}{99.5 \times 10^{-6} \times 8} = 10552.5\Omega$$

This is for an overdrive factor of 8. But the nearest standard value is $= 10K\Omega$

The oscillator frequency F, for IC3 is desired to be 800Hz.

From $F = \frac{1}{T}$, and $T = 1.1RC = 1.1 \times (1K + 10K) \times C$

$\Rightarrow T = 12100C$

Also F = 800Hz

$$\therefore C = \frac{1}{800 \times 12100} = 1.03 \times 10^{-7} \approx 0.1 \times 10^{-6} \approx 0.1uF$$

For transistor TR3, minimum $\beta = 60$

$I_E = 0.5A$ (Chosen value)

$$\Rightarrow I_B = \frac{I_E}{\beta + 1} = \frac{0.5}{60 + 1} = 8.2 \times 10^{-3} = 8.2mA$$

$$\Rightarrow R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{9 - 0.6}{8.2 \times 10^{-3}} = 1024.4\Omega$$

But the nearest standard value is $= 1000\Omega$

$\therefore R_B = 1K\Omega$

Hence, the construction of the digital quiz decider/timer device was based on the above design and analysis.

3.5 Construction

The construction of the digital quiz decider/timer device was done based on the design and analysis of the various segments. The following steps were taken for the full implementation of the construction.

3.5.1 Simulation

Simulation was the first step taken to ensure the workability of the design before the purchase of components. The simulation software used basically was the electrical work bench. The simulation was carried out in parts since attempts in simulating the whole circuit design did not yield the desired result.

3.5.2 Prototype

A model was made on the bread board before proceeding to the full implementation on Vero board. This was done in segments as well and then interconnected for the overall assessment of the performance. The desired results were obtained at this stage as well. Some of the apparatus/instruments used are;

- ▶ Multimeter
- ▶ Bread board
- ▶ Pliers/cutter
- ▶ Jumper wires
- ▶ Dry cells (9V and 5V)
- ▶ Components for the implementation

3.5.3 Implementation on Vero Board

The design was implemented on Vero board with a careful planning of the components layout. The planning was necessary to simplify wiring, minimize error, makes the implementation understandable on Vero board and makes troubleshooting easier. The following steps were taken;

- ▶ IC sockets were used to solder on the Vero board directly so as to avoid any damage to the ICs in the process of soldering. They were positioned to follow the circuit diagram after which the ICs were inserted.
- ▶ Adequate gaps were given between the ICs and components on the Vero board to reduce complexity.

▶The size of components on the Vero board was reduced to the bearest minimum to avoid short circuit. The IC pins were connected together with the aid of coated copper wires stripped at the ends and firmly soldered to the Vero board.

Tools and apparatus used during the full implementation includes

▶Vero board

▶Digital multi meter

▶Razor blade

▶Soldering iron and Lead

▶Lead sucker was used to remove de soldered Lead away from the board.

▶Pliers/cutter

▶Coated copper wire

3.5.4 Packaging

The packaging was done with a wooden material. The switching panel for the contestants was separated from the device while the RESET switch was placed on the device to be controlled by the quiz master. One seven segment display was placed in front of the quiz master while another was placed at the back of the device to be viewed by the contestants as well as the audience.

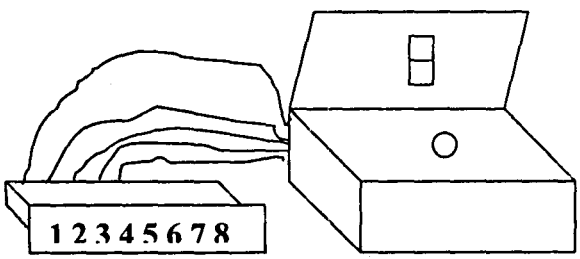

Fig 3.11 model package for the digital quiz decider/timer device

Chapter Four

4.1 Testing /Results Obtained

The following tests were carried out at different stages after full implementation of the design and the results were obtained appropriately.

▶The outputs of regulator ICs 7805 and 7809 for the power supply segment were measured with their outputs being 5V and 9V respectively as desired. Hence, the supplies to the selection and display segment as well as the alarm segment were as required. This avoided burnt of the components due to over voltage supply.

▶On power on, the display showed '0' since all the inputs are logic high. This was also the case whenever the device was reset.

▶After any of the switches (1-8) is pressed, the device latched such that it does not take any other input from the contestants until the reset button is pressed. Hence, the number of the switch pressed remained on the display until the reset button was pressed.

▶Immediately after a switch was pressed, the alarm sounded for 1second and stop and then started after 15seconds. This second alarm was continuous until the device was reset through the reset button.

4.2 Discussion of Results

The results obtained from different tests were the expected results. From the results, it was maintained that on power on, the display shows '0'. After any of the switches (1-8) is pressed, the number of the switch is displayed accordingly and an alarm sounds indicating to the quiz master and the audience the contestant that is to answer the question. The timer also starts automatically with an alarm indicating when the time elapses. The display can only be

cleared to '0' and the final alarm stopped by the quiz master through the reset switch. the device latches itself after taking the first input hence preventing a contestant with higher priority number from overriding the one in charge until a reset switch is pressed.

The results obtained were therefore the desired results with the device serving its overall purpose.

Chapter five

5.1 Conclusion

The aims and objectives of design and construction of digital quiz decider and timer device has been achieved. It was aimed at providing a means whereby a group of contestants in a quiz contest will equal opportunities under the same conditions of answering questions as a test of their intellect.

With this device, fairness to contestants in choosing the contestant that indicated to answer the question first as well as the time allotted for a question is inevitable. The man power required to organize a quiz contest is also reduced. This gives rise to higher level of organization in the show and hence, the best among the contestants will be known.

5.2 Recommendations

The following recommendations were therefore made to enhance and further enlarge the scope of this project.

► A 'D' transparent latch of more inputs and a priority encoder of higher inputs can be used to design for more than eight contestants.

►This device is recommended for use in primary and post primary schools, games show, and etc for quiz contest.

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