DESIGN AND CONSTRUCTION OF AN ELECTRONIC VOTING SYSTEM WITH DIGITAL DISPLAY

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A Thesis Submitted to the Department of Electrical and Computer Engineering, Federal University of Technology Minna

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Dedication

This project work is dedicated to my late brother; Mr. Peter Ejiga may his gentle soul rest in perfect peace and to Almighty God, my creator.

Declaration

I, **Ejiga David Eigege**, declare that this work was done by me and has never been presented elsewhere for the award of a degree. I also hereby relinquish the copyright to the Federal University of technology, Minna.

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Acknowledgement

I sincerely acknowledge God Almighty for making this day come to pass and for the success of this project work.

My profound gratitude goes to my project supervisor, Mr. O. D. Ahmed for his support despite his tight schedule. A big thank you to Mr. N. Salawu for all the selfless services rendered towards the completion of this project work.

I humbly acknowledge the untiring supports and prayers from my uncle and father, Hon. A. E. Ejiga and every member of the family. I appreciate my mother, Mrs. Aboh Ejiga for her love. I also acknowledge my uncle, Hon. Adah Ohepo Ejiga for his financial and moral supports and the entire Ejiga family for their love.

I deeply acknowledge the contribution of Mr. and Mrs. Enoch Ocheola for being there for me at the time I needed them most.

These acknowledgements will not be complete without mentioning my late brother Mr. Peter Ejiga may his soul rest in perfect peace. I shall not forget you, thanks brother.

Finally, I acknowledge everyone who in one way or the other contributed towards the completion of this project work and my studies. Special thanks to my Head of Department Engr. Musa Abdullahi, all my lecturers, all my classmates and to you my friends. God bless you all.

Abstract

Due to the ever-increasing population and coupled with insufficient voting system, election has become tedious and slow in this part of the world.

To be able to meet up with other countries with improved and efficient voting systems, the electronic systems must be adopted by this region for its voting process.

For this reason, I opted for the design and construction of an *Electronic Voting Device* as an introduction to the automation of the voting process in this region. If develop, it will help to check electoral vices and ease the task of counting and increase speed.

Table of contents

List of Figures

List of Tables

CHAPTER ONE

General Introduction

The essence of democracy is that everyone accepts the results of elections, even when they lose them. Elections allow the populace to choose their representatives and express their preferences for how they will be governed. Naturally, the integrity of the election process is fundamental to the integrity of democracy itself. And, unsurprisingly, history is littered with examples of elections being manipulated in order to influence their outcome[1].

The design of a "good" voting system, whether electronic or using traditional paper ballots or mechanical devices must be robust against a wide variety of potentially fraudulent behavior. A voting system must be comprehensible to and usable by the entire voting population, regardless of age, infirmity, or disability. Providing accessibility to such a diverse population is an important engineering problem and one where, if other security is done well, electronic voting system could be a great improvement over current paper systems.

1.1 Electronic Voting Systems

There have been several studies on using electronic technologies to improve elections.

As a result of several electoral rigging, the inadequacies of widely-used ballot voting systems have become well understood by the general population[1]. For this reason I opted for the design and construction of *Electronic Voting*

Systems with Digital Display. The voting system will help to completely eliminate paper ballots from the voting process, and ballot sorting and counting[2].

In the design and construction of *Electronic Voting System with Digital Display,* low cost materials and reliable operation where the primary factors of consideration. The system is designed in such a way that if the contact switch is pressed a pulse is generated by the 555 timer, this pulse which is a high clock is received by the counter (4029) IC. This signal is then transferred to the BCD to 7-segment decoder (4511) IC which will decode the signal and display the result in equivalent decimal number.

In order to ensure the correctness, and security of the system, pin 4 of the timer circuit is deactivated by making it low[3], this prevent the timer from generating pulses without the knowledge of whoever that is in charge. Also a latch pin was added to the system which will disable the decoder from displaying of vote until enabled by the polling official.

Proper design of this system will be able to take care of all the inadequacies recorded by the ballot voting systems.

The block diagram of the *Electronic Voting System with Digital Display* is illustrated in fig.1.1 below.

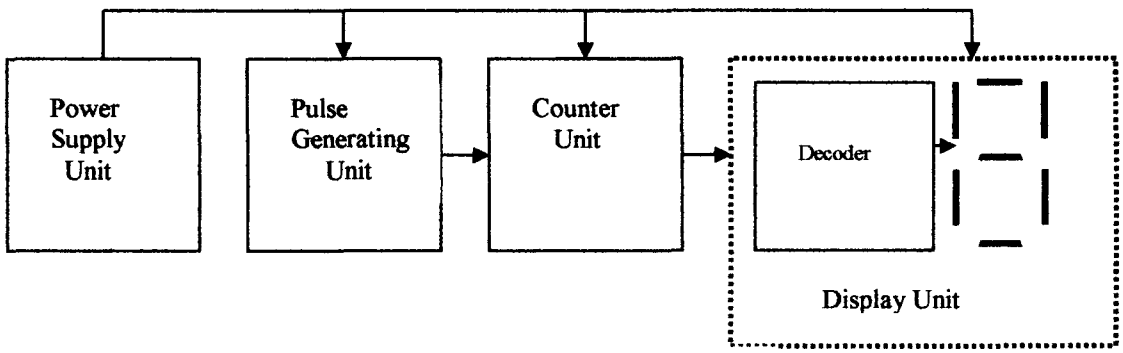

Fig. 1.1: Block diagram of *Electronic Voting System with Digital Display*

1.2 Aims/Objectives

The design and construction of *Electronic Voting System with Digital Display* is aimed at-:

i Introduction of automation in voting process to meet up with the challenges of the ever-increasing population of our societies.

ii Reducing fraudulent acts such as rigging and other electoral vices.

iii Eliminating errors due to counting since the votes will be display digitally.

iv It will help to ensure prompt and timely release of election results.

v Easing and reducing the task of polling officials during counting and evaluation of data and figures.

1.3 Methodology

The construction was carried out in three modules. The first module was the construction of the power unit on the bread board and then tested. The second module was the construction of the pulse generating circuit using 555 timer (IC) on the bread board and then tested. While the third module, was the construction of the counter and the displaying circuit. The 4029 IC was used as the counter while the 4511 IC was used as the decoder drive which convert binary signal from the 4029 counter into equivalent decimal number and display it. These components were connected on the bread board and tested.

1.4 Scope of Work

This project write-up is a report on the design, construction and testing of an *Electronic Voting System with Digital Display.*

Chapter one gives the general introduction of the project, objectives and the methodology of the project. Chapter two gives the literature review and the theoretical background of the project work. Chapter three gives the design and implementation, calculations and choice of components used. Chapter four gives the series of test carried out, the results obtained and the discussion of the result, and the shortcomings or limitations of the project work.

The last chapter gives the conclusion and recommendation for future improvement of the work done with reference to all the theoretical work.

1.5 Sources of materials

All the materials (components) used for the construction of this project were sourced locally from electronic vendors at the correct specifications and rating of the components.

CHAPTER TWO

Literature Review/ Theoretical Background

2.1 Literature Review

At the very beginning of ancient democratic government, we find Athens coming out to their open market square to cast votes by counting the numbers of people that raise up their hands in favor of a particular candidate[4]. The Ancient Greece citizens also adopted another method by using pieces of broken pottery to scratch in the name of the candidate in the procedures of ostracism. This was done because while parchment was expensive and had to be imported from Egypt, broken pottery was abundant and virtually free[7].

These processes continue until the population of people grows and becomes so large to handle. The open market square practice and the broken pottery practice became insufficient due to lack of space to accommodate or gather together all the people at a time and the task of counting which is bulky and tedious, leading to errors and some other fraudulent acts.

As a result of the insufficiency of these practices, the ancient democracy paved way to the contemporary institutions of democracy through open and secret balloting by the use of ballot box and papers. The first use of paper ballots to conduct an election appears to have been in Rome in 139 BCE[7]' and the first use

of paper ballots in North America was in 1629 within the Massachusetts Bay Colony to select a pastor for the Salem Church. Also the secret ballot was first introduced in Australia in the 1850s[7].

The secret ballot system is one of the most used in this part of the world. Although, is a highly adopted system, it has limitation in the area of sorting out and counting of total number of votes cast which is manually done, time wasting and late release of results.

The limitation of this balloting system coupled with the technological advancement led to the use of electronic devices as voting system/machine.

In advance countries such as America, some part of Europe etc, different system/machine has been in use. The system/machine ranges from punch card, direct recording electronic (DRE) system, optical scan voting system[1] etc.

The electronic voting systems have been in use since the 1960s[8] when punch card systems debuted. The newer optical scan voting systems allow a computer to count a voter's mark on a ballot. DRE voting machines which collect and tabulate votes in a single machine, are used by all voters in all elections in Brazil, and also on a large scale in India, the Netherlands, Venezuela, and the United States. Internet voting systems have gained popularity and have been used for government elections and referendums in the United Kingdom, Estonia and Switzerland as well as municipal elections in Canada and party primary elections in the United States and France[9].

This technological advancement has helped in automating and computerizing of voting process. So, many people have taken advantage of this development to come up with their own ideas and worked upon this topic. Different people with the combination of different circuitry have produced different voting systems/machines. For instance: the electronic ballot counter box[2], the unanimous vote counter machine[6] etc.

Therefore, it is on this basis that I opted to harness the use of pulse generating circuit, counter and decoder to synthesize an electronic system known as *Electronic Voting System With Digital Display* as an introduction to the automation of the voting process.

2.2 Theoretical Background

Theoretically, the *Electronic Voting System with Digital Display* is based on the principle of pulse generation. A monostable multi-vibrator is employed for the generation of this pulse[5]. The generated pulse which is an input clock, trigger the counter unit, making the counter(s) to count as many pulses that are generated. The counter unit then transmits this signal to the display unit. This unit is made up of the decoder/deriver and the 7-segment display. This unit is responsible for the conversion and display of the signal into visible readout.

Structurally, the system is a simple but highly efficient and reliable device; it makes use of low cost components which are locally sourced from the electronic vendors. In fact, the choice of the design and construction of this

particular voting system is due to the efficiency, reliability, availability and low cost of the components used.

The system is aimed at preventing electoral vices such as rigging, the bulky task of counting the total number of votes cast and the late release of election results and so on.

The principle upon which the system works is stated below;

When the contact switch is pressed, a pulse is generated by the 555 timer; this signal is received by the binary counter. The binary counter transmits the signal in the form of binary code to the BCD to seven segment decoder which then displays the signal into visible readout. Another pulse will be generated by the 555 timer at an interval of T= 1.1RC (seconds).

2.3 CONSTRAINTS

Several difficulties were encounter in the cause of this project work. Sourcing of materials 'on' and 'before' the commencement of this project work was an uphill task because; a lot of finance was spent on transportation to get the materials ready for the construction. Also a lot of money was spent sourcing for materials used in the write up of this project work.

Other problems were encountered during the construction process; some of the components used got damaged. It took me enough time to get them re-placed. The work was slowed down at this period. Also the constant power failure in the town was a serious problem faced during the construction and typing of this project work.

CHAPTER THREE

Design and Implementation

3.1 Power Supply Unit

The power supply unit comprises of the followings;

Power transformer circuit

Rectifier circuit

Filtering circuit

Power regulating circuit

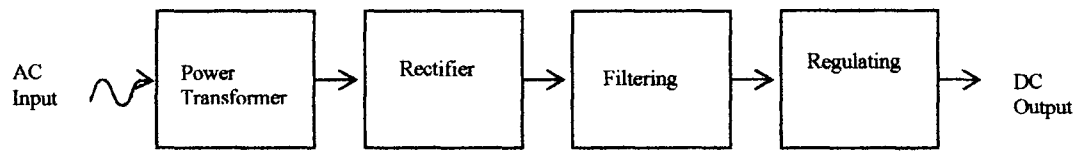

Fig. 3.1: Block diagram of power supply unit

3.1.1 Power Transformer Circuit

One of the major components in most AC power supply units is the power transformer[10]. The power transformer was used in this project as a step down voltages.

3.1.2 Step-Down Transformer

When the transformer primary coil turns are greater than the secondary coil turns, the voltage is stepped down and the current is stepped up in proportion to the turn's ratio, for an ideal transformer, $\mathbf{V_P \times I_P = V_S \times I_S}$

3.2 Rectifier Circuit

Rectification is the process of changing AC to DC. Diodes are commonly used as rectifiers in power supplies. There are two (2) major classifications of rectifier circuits: half-wave and full-wave. The full wave rectifier is employed in this project.

3.2.1 Full-Wave Rectifier Circuit

Since the half-wave rectifier makes use of only one half of the AC input wave, its uses is limited to low-power applications. Using a full-wave rectifier, a less pulsating and more powerful direct current can be produced by rectifying both half-cycles of the AC input wave.

The bridge rectifier circuit was chosen since it can be used in transformer-type as well as Line-operated power supplies; it also required no center-tapped transformer. The bridge rectifier circuit uses four (4) diodes to obtain full-wave rectification. As shown fig. 3.2: below

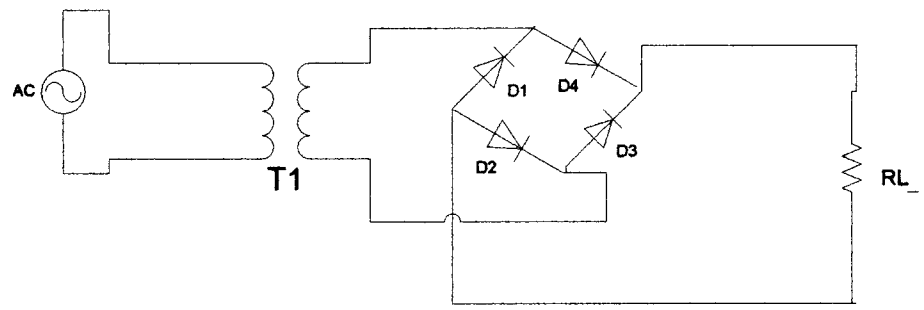

Fig. 3.2: The bridge rectifier circuit

CALCULATIONS

It is required to power the system with a 5V constant power supply. The 5V positive regulator IC, 7805 was used. The a.c mains voltage was step-down

by a 240/9V transformer, T_1 and rectified by a full wave bridge rectifier consisting of D_1, D_2, D_3, and D_4 as shown in figure 3.2 above. The rectified voltage is smoothening by capacitor C_1 and the resulting voltage is fed into a constant IC while a constant mains supply is obtained.

Since rms value of the transformer secondary winding is $9V_{rms}$

The peak value of the voltage, $\mathbf{V_P = \sqrt{2} x V_{rms}}$

$$\mathbf{= 9 \times \sqrt{2} = 12.7V}$$

For safe operation, the peak inverse voltage (PIV) rating if the rectifiers must be greater than V_{peak}. The diode IN4001 with PIV of 50V was chosen.

3.3 Filtering Circuit

A filter is used to reduce the amount of AC ripple, thus providing a relatively pure form of DC. This is because the pulsating DC output of the rectifier circuits is not smooth enough to properly operate most electronic devices. The main function of a filter circuit is to minimize the ripple content in the rectifier output as shown below

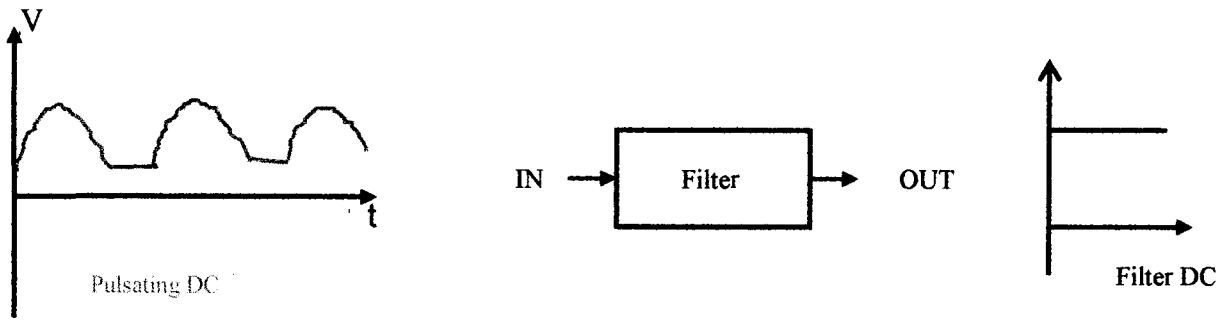

Fig. 3.3: AC component in a DC power supply

The most common filter device is a capacitor connected in parallel with the output of the rectifier circuit. The filter capacitor is a large value electrolytic capacitor. It makes an excellent filter because of its ability to store electric charges.

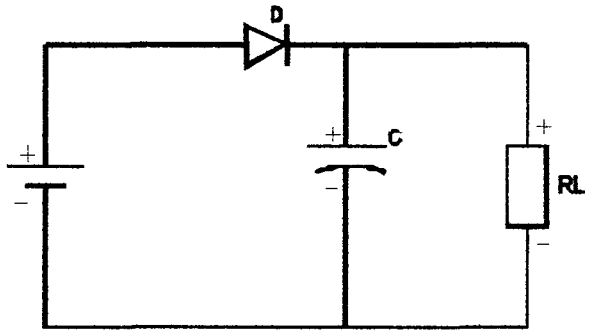

Fig. 3.4: Capacitor filter connection

CALCULATIONS

To calculate for the filtering capacitor, C

Recall, $\mathbf{C} = \dfrac{\mathbf{I}}{\{\mathbf{Fr} \bullet \mathbf{Vr}\}}$ [11]

Where **I** = the maximum load current

Fr = frequency of ripple voltage

Vr = allowable peak to peak value of the ripple voltage.

For a full wave rectifier, frequency of ripple voltage = 2x frequency of mains voltage.

Fr = 2f= 2x50 = 100Hz

I = 0.5A

Vr = 3V

Therefore, $C = \frac{0.5}{100x3} = 1.667x10^{-3}F$

$=1667x10^{-6} = 1667\mu F$

This is the minimal value of capacitance required. Its voltage rating must also be greater than Vpeak = **12.7V**

The value of 35V, 3300uF was chosen.

LED_1 is a power indicator and R_L is the current limiting resistor

$$R_L = \frac{Vs - Vd}{Id}$$

Where Vs = supply voltage

Vd = voltage drop

Id = current across the LED.

$$R_L = \frac{5-2}{3 \times 10^{-3}} = 1k\Omega$$

3.4 Power Regulating Circuit

A voltage regulator is an electrical regulator designed to automatically maintain a constant voltage level. It may use an electromechanical mechanism, or passive or active electronic components. Depending on the design, it may be used to regulate one or more AC or DC voltages. With the exception of shunt regulators, all modern electronic voltage regulators operate by comparing the actual output voltage to some internal fixed reference voltage. Any difference is amplified and used to control the regulation element. This forms a negative feedback servo control loop. If the output voltage is too low, the regulation element is commanded to produce a higher voltage. For some regulators if the output voltage is too high, the regulation element is commanded to produce a lower voltage; however, many just stop sourcing current and depend on the current draw of whatever it is driving to pull the voltage back down. In this way, the output voltage is held roughly constant. The control loop must be carefully designed to produce the desired tradeoff between stability and speed of response[12].

The power regulating circuit enables the power supply to maintain a constant voltage under varying input voltage or varying load current[10]. An IC voltage regulator was employed to provide the regulated power supply stability output voltages of 5V was regulated using 7805 IC voltage regulator with a permissible load current of 1A. The IC voltage regulator was mounted on a heat sink to radiate any excess heat out. In addition, a 1uF, 160V capacitor was fitted

to the output of the regulator to keep the output resistance of the circuit constant at high frequency.

3.5 Pulse Generating Circuit

Electronic timing circuits such as the popular 555 timer (an IC introduces as long ago as 1972) uses a pair of comparators, a flip-flop, and other components to generate a pulse whose length and duty cycle are controlled by an external RC network ranging from a few microseconds to several seconds[2]. Figure 3.5 below shows the internal structure of a 555 timer IC.

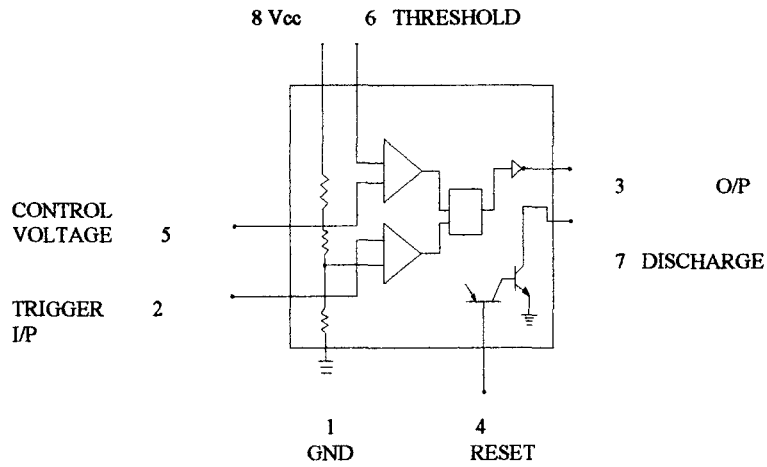

Fig.3.5: Detail circuit of a 555 timer IC.

3.5.1 555 Monostable

A monostable circuit produces a single output pulse when triggered. It is called a monostable because it is stable in just one state: 'output low'. The 'output high' state is temporary[13].

In this design, the popular NE555 Timer oscillator IC configured as a monostable timer is used. Its output at pin 3 would go high if the voltage at pin 2 falls below 1/3 of the supply voltage.

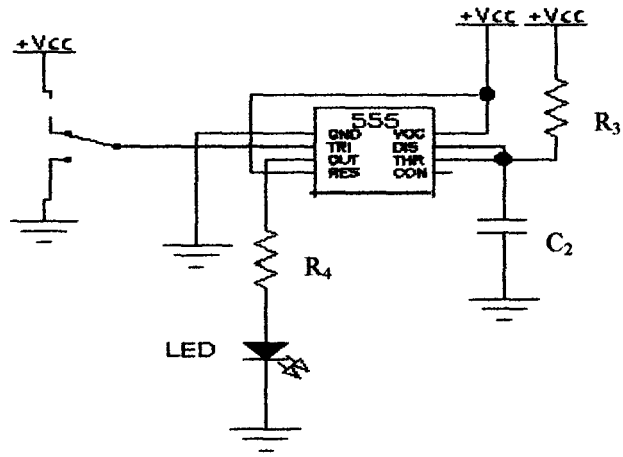

Fig. 3.6:NE555 timer Monostable operation

CALCULATIONS

The duration of the pulse is called the time period (T) and this is determined by resistor R and capacitor C.

Time period, $\mathbf{T = 1.1 \times R \times C}$

T = time period in seconds (s)

R = resistance in ohms (Ω)

C = capacitance in farads (F)

Where $R = R_3 + R_4$

$C = C_2$

Since $R_3 = 100k\Omega$

$R4 = 1k\Omega$

$\mathbf{R = 100 + 1 = 101k\Omega}$

The desired time period = 10seconds.

Therefore, $\mathbf{C = \frac{T}{1.1RC} = \frac{10}{1.1x101x10^3}}$

$$\mathbf{= 9x10^{-5}\mu F = 90\mu F}$$

But the nearest standard value of **C = 100μF**

The 1.1 in the time period was used because the capacitor charges to $^2/_3$ = 67% so it is a bit longer than the time constant $\{(R_3+R_4) \times C_2\}$ which is the time taken to charge to 63%.

3.5.2 Monostable Operation

The timing period is triggered when the trigger input (555 pin 2) is less than $^1/_3$ Vs, this makes the output high (+Vs) and the capacitor C_2 starts to charge through resistor (R_3+R_4). Once the time period has started further trigger pulses are ignored.

The threshold input (555 pin 6) monitors the voltage across C_2 and when this reaches $^2/_3$ Vs the time period is over and the output becomes low. At the same time discharge (555 pin 7) is connected to 0V, discharging the capacitor ready for the next trigger.

The reset input (555 pin 4) overrides all other inputs and the timing may be cancelled at any time by connecting reset to 0V, this instantly makes the output low and discharges the capacitor. If the reset function is not required the reset pin should be connected to +Vs.

3.5.3 Power-On Reset or Trigger

It may be useful to ensure that a monostable circuit is reset or triggered automatically when the power supply is connected or switched on. This is achieved by using a capacitor instead of (or in addition to) a push switch.

The capacitor takes a short time to charge, briefly holding the input close to 0V when the circuit is switched on. A switch may be connected in parallel with the capacitor if manual operation is also required. This arrangement is used for the trigger in the Timer Project.

3.5.4 Edge-Triggering

If the trigger input is still less than $^1/_3$ Vs at the end of the time period the output will remain high until the trigger is greater than $^1/_3$ Vs. This situation can occur if the input signal is from an on-off switch or sensor.

The monostable can be made edge triggered, responding only to changes of an input signal, by connecting the trigger signal through a capacitor to the trigger input. The capacitor passes sudden changes (AC) but blocks a constant (DC) signal. The circuit is 'negative edge triggered' because it responds to a sudden fall in the input signal. The resistor between the trigger (555 pin 2) and +Vs ensures that the trigger is normally high (+Vs).

3.6 Counting Circuit

One of the most common requirements in digital equipment is counting. And the most common counting requirement has to do with time. From a basic digital clock (which is incorporated into most digitally-controlled appliances) to interval timers and event counters, the need for counting circuits is very great.

Counters are required for various counting ranges and in all sorts of circumstances. A simple digital clock, for example, requires a decimal counter for the units positions of seconds and minutes, but must count only from 0 to 5 (modulo-6) for the tens positions of minutes and seconds. Hours digits require special handling, since the two-digit output must count either from 1 to 12 or 0 to 23, depending on how we want the display to appear. Some clocks skip the 0 to

23 military displays and run from 1 to 24 in that mode. And some simple clocks make no effort at that, or to distinguish between AM and PM.

No matter how the hours are handled, the basic element required to make any digital clock work is the counter circuit. Indeed, counters are so important in so many applications that many different kinds of counter ICs have been designed for both TTL and CMOS logic families. Some count up for clocks and time intervals; others count down to show time remaining until some event. Some are specifically designed to count in decimal mode, while others count in binary, and still others have selectable counting ranges.

Electronic circuits count in binary. This is the simplest possible counting system because it uses just two digits, 0 and 1, exactly like logic signals where 0 represents false and 1 represents true. The terms low and high are also used for 0 and 1 respectively as shown in the table below.

Table 3.1: Truth table of the binary counter

Logic	True	1	High	+Vs	On
States	False	0	Low	0V	Off

All counters require a 'square wave' clock signal to make them count. This is a digital waveform with sharp transitions between low (0V) and high (+Vs), such as the output from a 555 monoastable circuit[15]. The 4029 CMOS counter IC was used in the construction of this project

3.6.1 The 4029 CMOS Counter IC

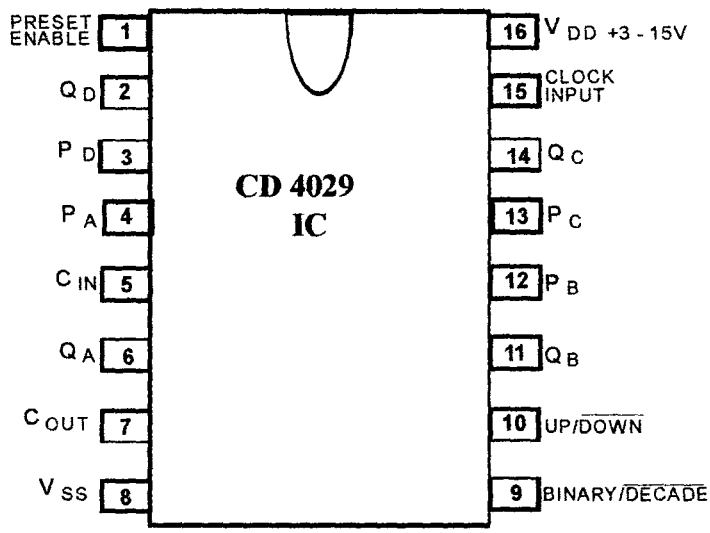

Fig. 3.7: Functional diagram of a CD 4029 up/down counter

The internal schematic diagram of the 4029 is quite complex, as it involves a gating structure that will allow counting up or down, in binary or decimal, and with parallel inputs to preset a count. However, we can't reach the internal circuitry in any case, so the functional diagram is far more useful for our purposes.

Most of the designations are straightforward and intuitive. The up/down input, for example, tells the counter to count up if it is a logic 1, or down when it is logic 0. In the same way, logic 1 to the binary/decimal input causes the counter to operate in binary mode, while logic 0 switches it to decimal (sometimes called *decade*) mode. If multiple 4029s are cascaded for a larger count, all up/down pins are connected together and driven from a common signal, as are all binary/decimal lines.

The C_{IN} and C_{OUT} lines form the means of cascading counters and still keeping a fully synchronous count. If C_{IN} is logic 1, the counter won't count at all. When C_{IN} goes to logic 0, the counter operates normally. Then, when the counter reaches its terminal count (9, 15, or 0 depending on the states of up/down and binary/decimal), C_{OUT} goes to logic 0. This is connected to the C_{IN} line of the next IC to allow the next higher order of magnitude to count once. Then C_{OUT} goes to logic 1 again. The first counter IC in the set, representing the least significant digit, has its C_{IN} line grounded to logic 0 so it will always count.

The clock input, like up/down and binary/decimal is fed to all 4029s in an extended counter circuit. This is the signal that represents whatever is to be counted. Any 4029 that is enabled by having its C_{IN} line at logic 0 will change state to the next count when the clock rises from logic 0 to logic 1. Any changes to the C_{IN} and C_{OUT} lines will occur just after that rising edge, and so will be ready for the next clock pulse.

The input is the preset enable line, and is also shared with all 4029s in the counting set. When this line is logic 0, the counter operates normally. However, when becomes logic 1, the logic signals present on the four jam input lines get copied directly to the four bits of the counter, overriding any prior count. These inputs are not always used, and many applications ignore them. However, there are some applications that do use these inputs to advantage. For example, if we want to count for a multi-digit interval in seconds, we can set the jam inputs to the decimal number of seconds to be counted and configure the circuit to count down.

When the counter reaches zero, the final C_{OUT} line falls to logic 0 and can be used after inversion to preset the count again to the selected number, or to stop the count and signal the end of the timing interval.

The four outputs, of course, are the current count as either a binary or BCD number, depending on the state of binary/decimal. Output 1, often designated, Q_D is the Least Significant Bit (LSB), while output 4 (or Q_A) is the Most Significant Bit (MSB).

Table 3.2: Gives the four outputs of the 4029 Counter IC

Decimal	**Binary Equivalent**			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

All inputs and outputs are standard CMOS design, and operate in the normal manner for CMOS ICs. The 4029 is specified to operate accurately for clock signals up to 2 MHz minimum. And typically 4 MHz, with a 5 volt power supply. It will run faster with higher power supply voltages.

3.6.2 Linking Counters

Counters may be linked together in a chain to count larger numbers. A 12-bit or 14-bit counter may be used directly, but it is not practical to convert their large binary numbers to decimal. It is more easier to use a chain of decade (0-9) counters which use BCD (binary coded decimal) to make the conversion to decimal very easy: the first counts the units, the second counts the tens, the third the hundreds and so on.

Some dual counter ICs are available with two separate counters on the same IC, the two counters must be linked externally if required (there is no internal link). The way that counters are linked depends on the nature of the counter.

3.6.3 Linking Synchronous Counters

The diagram below shows how to link standard synchronous counters. Notice how all the clock (CK) inputs are linked, and carry out (CO) is used to feed the carry in (CI) of the next counter. This ensures that the entire counter chain is synchronous, with every output changing at the same time.

Carry in (CI) of the first counter should be made low or high to suit the particular counter IC being used.

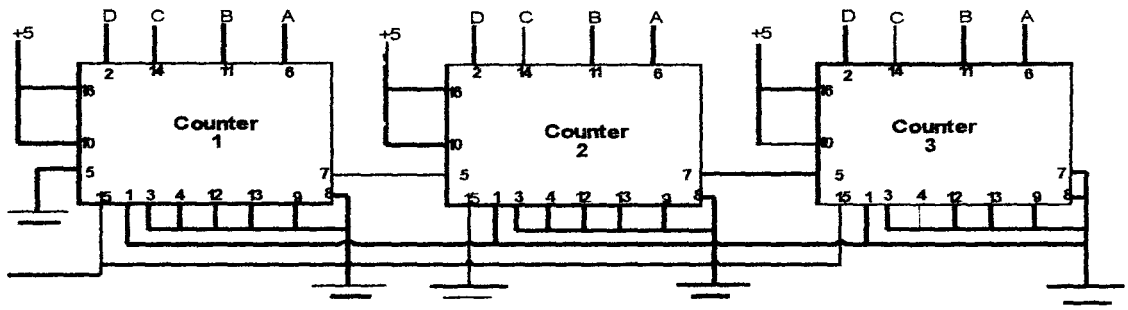

Fig. 3.8: Diagram showing linking of synchronous counters

3.7 Decoder Circuit

The most popular type is a 1-of-10 decoder which contains a network of logic gates to make one of its ten outputs Q_{0-9} become high (or low) in response to the BCD (binary coded decimal) inputs A-D. For example an input of binary 0101 (= 5) will activate output Q_5. Decoders can be used for a simple counting display and for switching LEDs in sequences.

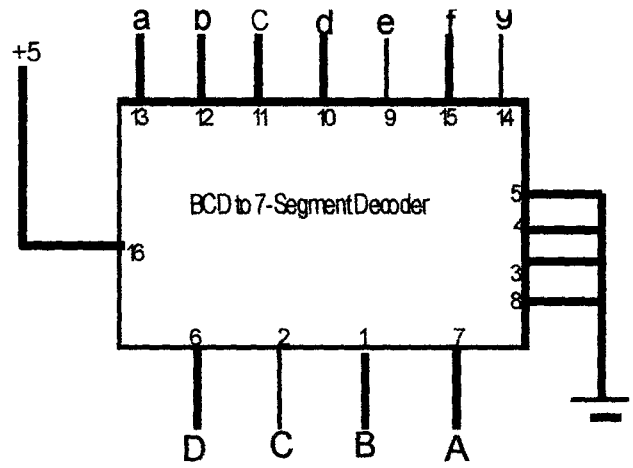

Fig. 3.9: Circuit Diagram of a BCD to 7-Segment decoder

In this project work, three (3) independent BCD to 7-segment decoder units were used. The binary outputs from the counter are fed to the binary inputs of the ICs (CD4511) and appropriates outputs of the 7-segment display is force to go high or low which corresponds to the decoded binary inputs. The truth table for the operation is given below.

Table 3.3: Truth table for the operation of BCD to 7-segment decoder

Decimal	Binary Coded Decimal (BCD) Count				7-segment Output						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	1	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	0	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	0	0	1	1

3.7.1 Operation of CD 4511 7-segment Decoder\Deriver

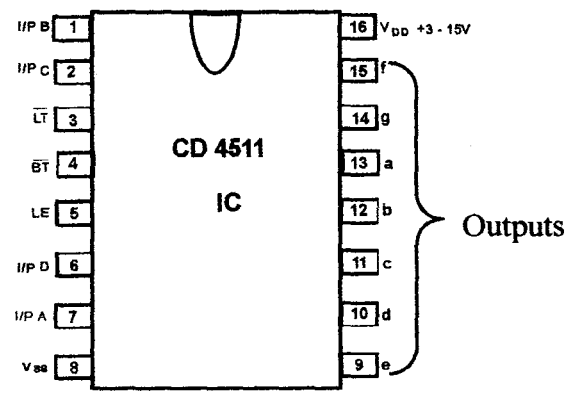

Fig. 3.10: Functional diagram of a CD4511 BCD to 7-segment decoder

LT (pin 3) is the lamp test for normal operation, this pin is connected to ground should it be taken high, all the seven segment outputs would go high irrespective of the present count. BT (pin4) is the blank test. It is active low and thus should be kept high for normal operation, should this pin go high all the 7-segment outputs would go low. This creates a blank display for a common cathode display. LE (pin5) is the latch enable. It is active high therefore it should be low for normal operation. If pin5 goes low the count on the 7-segment display would be latched irrespective of further changes in the BCD inputs.

3.7.2 7-Segment Display Unit

The inputs A-D of a display driver are connected to the BCD (binary coded decimal) outputs Q_{A-D} from a decade counter. A network of logic gates inside the display driver makes its outputs (a-g) become high or low as appropriate to light the required segments (a-g) of a 7-segment display. A resistor is required in series with each segment to protect the LEDs, 330Ω is a suitable value for many displays with a 4.5V to 6V supply.

There are two types of 7-segment displays: Common Anode (CA or SA) with all the LED anodes connected together. These need a display driver with outputs which become low to light each segment, for example the 7447. Connect the common anode to +Vs.

Common Cathode (CC or SC) with all the cathodes connected together. These need a display driver with outputs which become high to light each segment, for example the 4511. Connect the common cathode to 0V.

The common anode/cathode is often available on 2 pins. Displays also have a decimal point (DP) but this is not controlled by the display driver. The segments of larger displays have two LEDs in series.

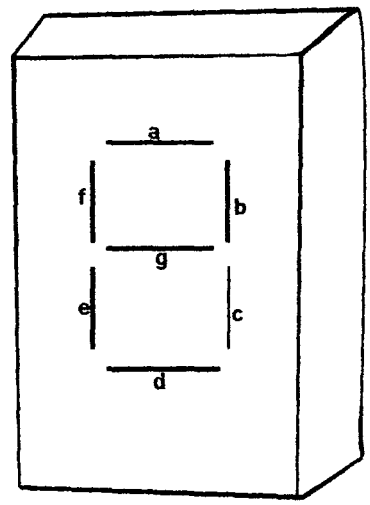

Fig. 3.11: Diagram of common cathode 7-segment display

CHAPTER FOUR

Tests, Results and Discussion

4.1 Tests

Each of the constituting units of the device being constructed were simulated one after the other before being tested on project board (bread-board) and then finally soldered to the main Vero-board.

The *Electronic Voting System with Digital Display* was tested to make sure that each pulse generated is being counted by the counter and equally decoded by the decoder/deriver. Also, it was ensure that the decoded signal was display in a visible readout by the 7-segment display.

Finally, the deactivating pin (pin 4) of the pulse generator was tested to make sure that it was able to hold the timer from generating unwanted pulse and pin 4 of the decoder/deriver circuit was tested to make sure that it provides a blank screen even when count is still on.

4.2 Results

The results obtained during testing are tabulated as follows;

Table 4.1: Gives the results of the test carried out

Number of vote(s)	Screen Display
1 – 9	001 – 009
10 – 99	010 – 099
100 – 999	100 – 999
1000	000

4.3 Discussion of result

The design of this project was aimed at casting of vote(s) with an equally display of such vote(s) as soon as it is cast.

When the contact switch is pressed between one to nine times, the first counter counts and then send the signal to the BCD to 7-segment decoder\deriver which decode and transmits the signal in decimal equivalent to the display unit which displays it on the screen as(001- 009). At the tenth to ninety ninth press, the second counter became active and the equivalent count was display on the screen as (010 -099). The third counter became active at the hundredth to nine hundred

and ninety ninth press of the contact switch, the screen display (100 -999). Finally, the display reset back to 000 at the count of one thousand.

CHAPTER FIVE

Conclusions

The target of this project which is "design and construction of an *Electronic Voting System with Digital Display*" was achieved as demonstrated by the results obtained from the test carried out as explained in chapter four

My aim which was to use an electronic system rather than the traditional ballot box and paper in voting process was achieved. This is an improvement in the electioneering process of Nigeria and this part of the world.

Though, a number of difficulties were encountered at the design and construction stage of this project, due consultation and constant research help me to get through.

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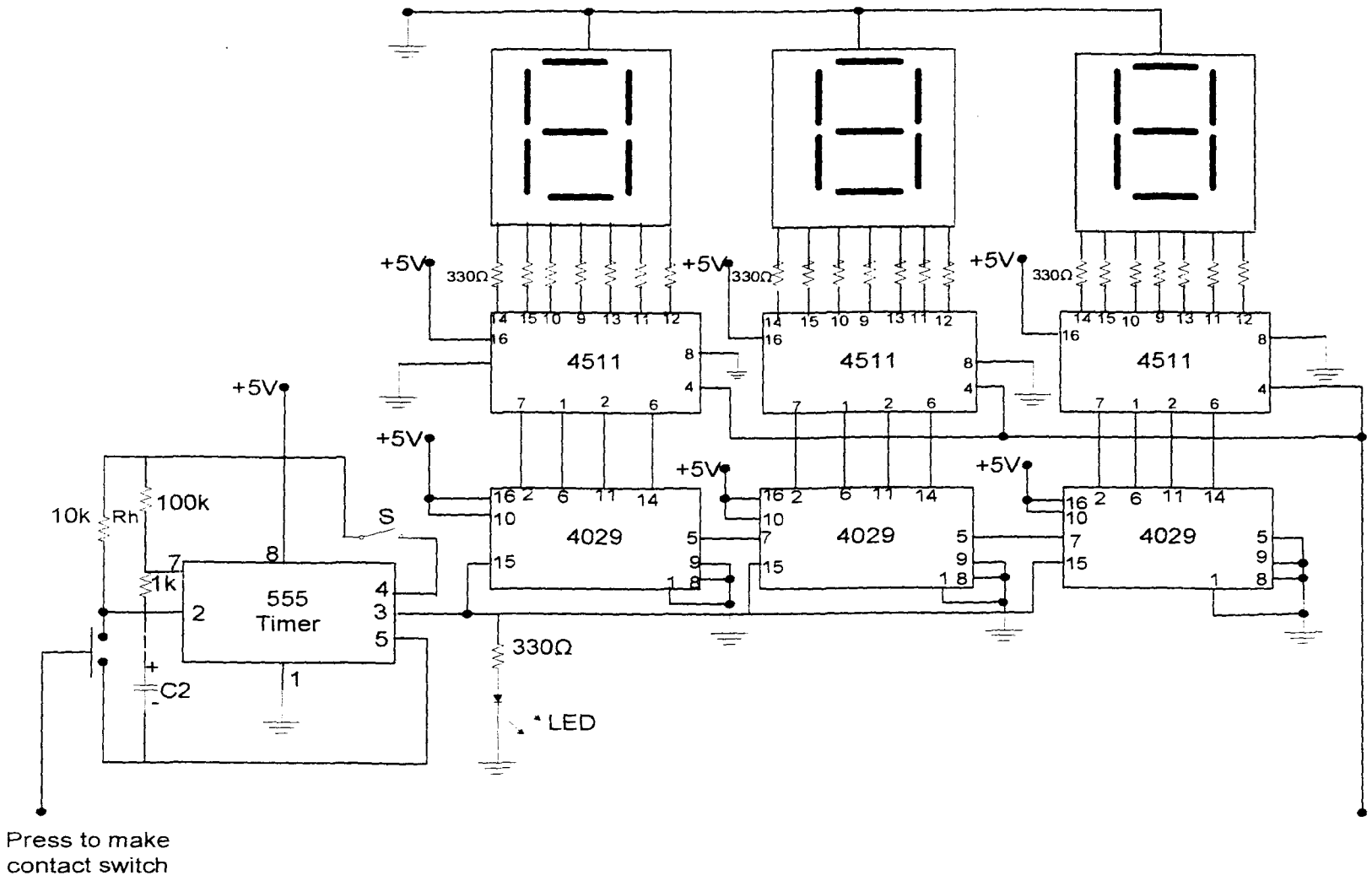

Circuit Diagram of Electronic Voting System with Digital Display