DESIGN AND CONSTRUCTION OF A MICROCONTROLLER BASED DIGITAL ELECTRONIC VOTING BOX

BY

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DEDICATION

This project work has been dedicated to my late father (Alh. Aliyu Guyegi) who died as at when his services were most needed.

Declaration

This is to certify that this project titled "Design and construction of a microcontroller based digital electronic voting box" was carried out by ALIYU A NMA under the supervision of Engr. M.S. Ahmed and submitted to Electrical and Computer Engineering Department, Federal University of Technology, Minna for the award of Bachelor of Engineering (B.ENG) degree in Electrical and Computer Engineering.

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ABSTRACT

Little or no technological advancement with geometric increase in population couple with manual ballot counting has made a democratic system practice by underdeveloped countries of world inefficient, slow and unattractive. Nigeria falls into the league of such countries which democratic system makes uses of manual ballot counting.

To move away this archaic system and join other countries like America, Britain, and even south Africa which democratic system are advanced, technology must be adopted to automate democratic process in Nigeria.

It is on this I thought it wise to design and construct a MICROCONTROLLER BASE DIGITAL ECLECTRONIC VOTTNG BOX as an improvement to the automation of electoral process in Nigeria which if developed and delivered to the appropriate electoral agency will help curtail electoral vices and ease the task of counting and increase efficiency and speed.

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CHAPTER ONE

1.1 INTRODUCTION

All over the world, democracy has come to stay as the major and most recognized tool of governance. Democracy is defined as a government of the people by the people and for the people. In practice, it is merely a government by the majority [4]. To realize this form of government, some democratization processes are involved which are handled by an electoral body constituted solely for the job.

The processes involve formation and registration of political parties' delineation of electoral district, compilation of voters register and, most importantly, the electioneering and counting of votes. The electioneering and counting of votes are the most tasking and sensitive part of the democratization process, especially when the manual counting system is in use. This is more hectic in a situation where rapid population growth is astronomical. This in effect has made the manual counting of votes tedious, bulky and erroneous which most often than not leads to electoral vices such as thuggery and rigging.

Therefore, the automation of democratization process in Nigeria has become inevitable or else, she will find it difficult to meet up the challenges of the new era as seen in the ever increasing population of the nation. The design and construction of a microcontroller based digital electronic voting box which is also an automation of electoral process will help in reducing the fraudulent acts, easing and reducing the task of counting and evaluation and, in addition ensuring prompt release of electoral results.

1.2 Aim and Objectives

The design and construction of a microcontroller based digital electronic voting box is aimed at

i. Reducing fraudulent acts such as rigging and other electoral vices at the poling collation centers by actually, knowing the total number of votes cast during any election.

ii. Easing and reducing the task of polling masters during counting and evaluation of data and figure as the counters display the exact value of vote cast and to which individual party was it for.

iii. Improving on automation of voting process to meet up the challenges of the new millennium as seen in the ever increasing g population of any politically defined nation.

iv. To ease and promote the effective use of error free data which could be collected by reputable world organization such as W H.O, UN, OAU, and so on.

v. Reducing the time taking before elections results are released.

1.3 Motivation

Nigeria stands as the giant of Africa and should lead in all field of life including its electioneering process, this cannot be achieved in the way and manner in which election are held in Nigeria with lots of irregularities, this motivated me into designing and construction of a microcontroller based digital electronic voting box which will Insha Allah solve the irregularities faced during voting.

1.4 Methodology

This design made use of the variation in electrical property of a semiconductor device with respect to the light intensity falling on it. Such devices are called photo detective devices; for the purpose of this design a light dependent resistor was used. The output from the photo detective device is fed into a quad voltage comparator (LM339) which compares the voltage with a reference voltage and subtracts it out to produce a zero output, this output was fed to inverter which Inverts the signal for the microcontroller, the microcontroller then make the decision according to the perforation on the card, it produces pulses at its output pin which are being fed into a seven segment drivers which drives the display. The microcontroller is also responsible for the control of an electromagnetic slot, that is, it opens for the card to fall and close it up back with the help of springs.

1.5 Scope and Limitation

This design counts ballot papers from 1 – 999 at four different display units, the displays are for

a) Total vote caste.

b) Party As vote.

c) Party Bs vote.

d) Invalid votes.

Provision for back up battery was not made hence it should be supplied with a constant power supply to avoid interruption during election.

1.6 **Source of Information**

Information which helped in achieving this design was sourced from different sources; they include Text books, the Internet, Lecture note and past projects. Lecturers were also consulted during the design of the project.

CHAPTER TWO

2.1 LITERATURE REVIEW

At the very beginning of ancient democratic government, we find Athens coming out to their open market square to cast votes by counting the number of people that rinse up their hands in favor of a particular candidate [4].

As the population of people grows and becomes so large to handle through open market square practice, the ancient democracy gave way to the contemporary institution of democracy through open and secret balloting by the use of ballot box and cards.

In recent times, the manual ballot box has proved to be inefficient due to the ever increasing population of human kind and technological advancement in medicine, health, food research, hygiene, etc which has drastically reduced mortality rate, increased birth rate and qualitative and quantitative improvement in man's live time. Previous work on this field include the design and construction of a digital electronic ballot counter box by Lasisi Lawal, final year project 2000 (Department of Electrical Computer Engineering FUT Minna)supervised by ENGR.M.S. AHMED. His design aimed at getting the total vote cast during election.

That same technology has to be harnessed to automate and computerization process to help meet up with the challenges of the new millennium as I chose to use optoelectronic device, inverting circuit, decision circuit and electromagnet to synthesize an electronic system known as Microcontroller based digital electronic voting box as an improvement to the automation of democratization process. This design will not only display the total vote cast but will also differentiate to which political party the vote was casts for between two political parties, also provision for invalid vote was made.

2.2 Theoretical Background

This design uses the photo dependent properties of semiconductors, the light dependent resistor is the photo detector used in this design, circuitry component uses to achieve the entire design include, light emitting diode, Quad comparator LM339, inverter, Microcontrollers (AT89C52 and AT89C2051), seven segment display, electromagnet.

2.21 Light dependent resistor

A Light Dependent Resistor also known as LDR, photoconductor, or photocell is a device which has a resistance that varies according to the amount of light falling on its surface. A typical light dependent resistor usually has a resistance in total darkness of 1 MOhm, and a resistance of a couple of 1kOhm in bright light (*10-20kOhm @ 10 lux, 2-4kOhm @ 100 lux*). They are used as light/dark activation switches depending on the way they are connected in circuit.

2.22 Voltage comparator (LM339)

The LM339 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.
Application areas include limit comparators, simple analog to digital converters; pulse, square wave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM339 series was designed to

directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic. For the purpose of this design it is used to subtract the voltage coming out from the LDR from a reference voltage, at certain darkness on LDR the out put from the LM339 will be a zero. Three out of four of the Quad comparator was used and are directly connected to three LDR.

2.2.3 7404 Inverters

The 7404 is an integrated circuti that converts what ever comes to its input pin to its opposite, logically it is called Not gate. The 7404 is equiped with six not gate, it has a large operating voltage range making it useful in various circuits, it also uses a low input current and has a high Noise immunity capacity. Outputs can directly be Interface to CMOS, NMOS and TTL which makes it very useful in out design and was interfaced directly to the input pins of our decision.

2.2.4 Microcontrollers

A microcontroller programmable integrated circuit that is usually programmed to control a specific task. The microcontrollers used for this design are the AT89C52 and the AT89C2051,

The AT89C52 is a 40 pin microcontroller which provides the following standards: 8K of flash, 256 bytes of RAM, 32110 lines, three 16-bit timer counters, a six-vector two level interrupt architecture, a full duplex serial port, on chip oscillator, and circuitry. For the purpose of this design port 1 was used as input and port 0 for output. The AT89C2051 is a 20 pin microcontroller which provides the following standards: 2K bytes of Flash, 128 bytes of RAM, 15 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt

Architecture, a full duplex serial port, a precision analog comparator, on-chip oscillator and clock circuitry. In addition, the AT89C2051 is designed with static logic for operation down to zero frequency and supports two software selectable power saving mod. For the purpose of this design it it used as a multiplex driver for the 3*7 segment displ y.

2.2.5 Seven segment display

This is simply the arrangement of light emitting diode in pattern that can be used to show numerals, the LED is an electro luminescent system that emits light when a voltage in applied to it. They come in either common anode been an active low or common cathode been active high, for this design we chose the common anode connection.

2.2.6 Electromagnet

This is a temporary magnet caused by the passage of current through a coil, it losses its magnetism immediately when the coil is de energized. For the purpose of this design an electromagnet was incorporated with the slot to open up any time a vote is casted so that the card fall off and close up so as to block the slot thus, getting ready to accept an incoming card

CHAPTER THREE

3 1 Design and Implementation

This section will give a through description of the design and how it is constructed. The design consists of seven basic units which are as follows:

i. The power supply

ii. The light source and photo sensing unit

iii. Voltage comparating unit

iv. The Inverting Unit

v. The decision unit

vi. The display drivers and display unit

vii. The electromagnet unit

Below is a block diagram of how the various units are interconnected.

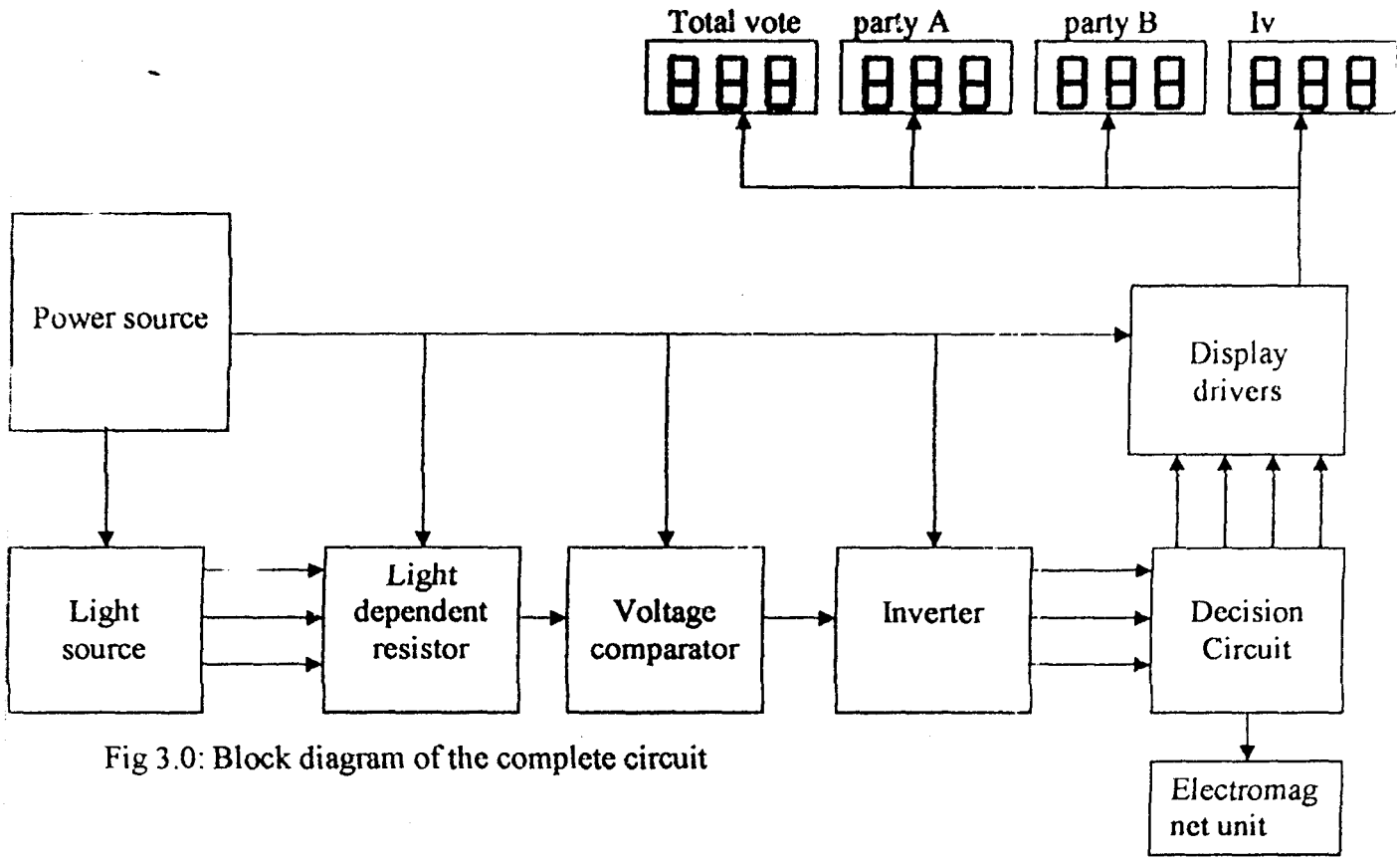


Fig 3.0: Block diagram of the complete circuit

3.2 Power supply Unit

Almost all electronics uses direct current for operation and the most convenient and economical source of power is the domestic alternating current supply where alternating voltage (220 $V_{r.m.s}$) is stepped down to a desired voltage and converted to DC voltage. This process is known as rectification and is achieved with the use of rectifiers (diode), filters (electrolytic capacitor) and voltage regulators to help maintain a constant voltage across the load.

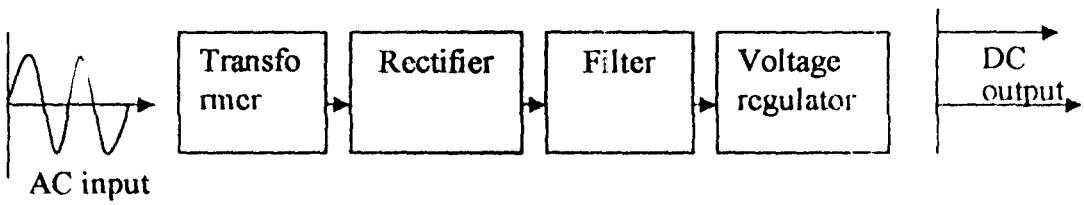


Fig 3.1 Block diagram of a regulated power supply

3.2.1 The Transformer

This is a device used to either step down or step up voltages, for the purpose of our design we require a step down transformer.

Design factor from output to input = 1.8

Output voltage (Regulated) = 5V and 6V

Regulator input = 5 x 1.8 = 9V and 6 x 1.8 = 10.8

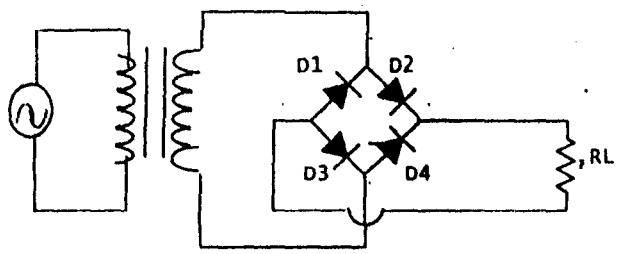
V_{max} = for our design factor = 10.8

V_{rms} = 0.707 x 10.8 = 7.636

With this value as input to the regulator, the preferred value of stepped down transformer to make up for low voltage supply is 12V, therefore, the transformer used in the design is a 220/12, 1000mA step down transformer.

3.2.2 **Rectifying circuit**

This is a circuit which converters an AC voltage to a DC pulsating voltage, it is achieve by arranging diode in a certain way, our design aimed at achieving full wave rectification uses four diodes arranged in a pattern known as a bridge rectification, bridge rectifier has four diodes arranged in such a way that AC enters through joined positive and negative terminal and the output has its polarity being positive where two negative terminal joined and negative where two positive terminal joined, the arrangement is as shown below



D1-D4 IN4007

Fig 3.2 Bridge rectification of

In choosing rectifier for design purposes, it is very important to know the peak inverse voltage (PIV) that appears across the diodes.

$V_{d.c} = \frac{2V_{max}}{\Pi} = 0.636\ V_{max}$ ....(1)

$PIV \geq V_{max}$

$V_{rms} = 12V$

$V_{max} = \sqrt{2}\ V_{rms} = 16.917$

Allowing a safety margin of 1.5

$V_{max} = 1.5 \times 16.971 = 25.457$

$V_{max} \approx 25V$

2A bridge rectifier with peak reverse voltage of 200V was selected

3.2.3 Filtration Circuit

After the incoming stepped down Ac voltage passes through the bridge rectifier it is turned to a pulsating Dc which has to undergo filtration to be pure for use is the circuit. Diagram below illustrate the process

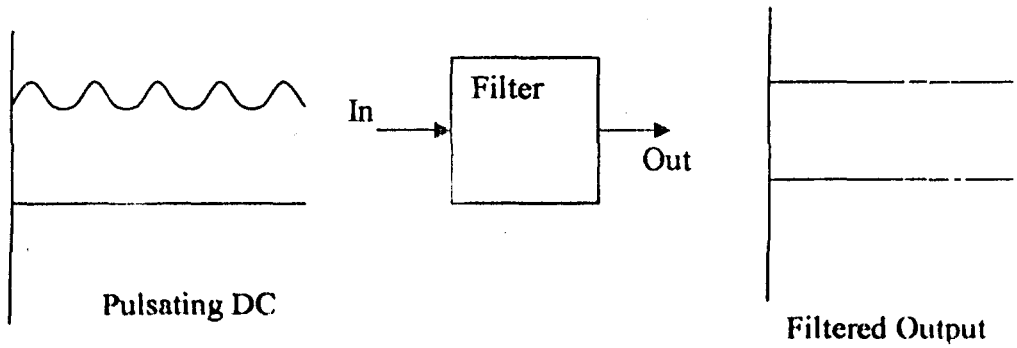


Fig 3.3 Block diagram of filtering action

The ripple voltage can be approximated by triangular waveform which has a peak to peak value of Vr (P-P) and a period of Tr

Charge lost dq in time T is IdcTr

$$Vr\,(P\text{-}P) = \frac{\delta Q}{C} = \frac{ITr}{C} = \frac{Vdc}{FrCR_L} \quad \ldots\ldots (2)$$

$$Vr(r.m.s) = \frac{Vr(P\text{-}P)}{2\sqrt{3}} = \frac{Vdc}{2\sqrt{3}\,FrCR_L} \quad \ldots\ldots (3)$$

$$\text{Where } \gamma = \frac{Vr(r.m.s)}{Vdc} = \frac{1}{2\sqrt{3}\,FrCR_L} \quad \ldots\ldots (4)$$

For full wave rectifier Fr = 2f where f is the line frequency and Fr is the ripple frequency

$$\gamma = \frac{1}{4\sqrt{3} \times FrCRL} : R_l = \frac{V_{max}}{Idc} \quad \ldots\ldots (5)$$

$$\text{Therefore } \gamma = \frac{Idc}{4\sqrt{3} \times FrCV_{max}}$$

γ is to be kept at minimum (0.0386)

$$C = \frac{Idc}{\gamma \times 4\sqrt{3} \times FrCV_{max}}$$

Where $\gamma = 0.0386$

$F = 50Hz$

$V_{rms} = 12V$

$V_{max} = \sqrt{2}V_{rms}$

$Idc = 0.5A$

$$C = \frac{0.5}{0.0386 \times 4\sqrt{3} \times 16.971 \times 50}$$

$C = 2203 \times 10^{-3}$ which is approximately 2200μF

Hence capacitor of value 2200μF was chosen for the filtration

3.2.4 **Regulating circuit**

The regulating circuit enables the power supply to maintain a constant voltage to the load circuit IC voltage regulator was employed for regulation, our design made use of the 7805 and 7806 voltage regulators to respectively produce 5V and 6V regulated output. The complete circuit of the power supply is as shown below.

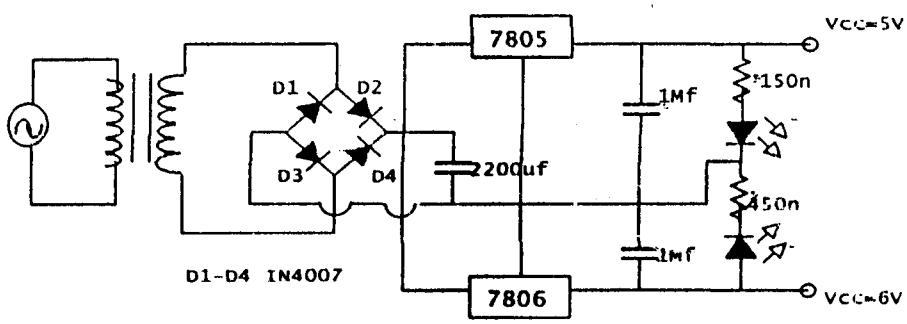


Fig 3.4 Complete circuit diagram of power supply

3.3 Light source and photo sensing unit

3.3.1 Light Source

This design depends highly on light being transmitted continuously in short range where ambient temperature and penetrating power are not problems. A white colored led is used as the light source and is placed at a short distance very close to the light dependent resistor. Three of the light emitting diode in number arranged closely opposite to three light dependent resistors.

Led is a PN junction diode that emits light when forward biased. They were connected with a limiting resistor so as to minimize current flowing into them. The limiting resistor value is obtained below

$V_{cc} = I_{led}R + V_{led}$ .....(6)

Where V_{led} = Voltage drop across LED = 2V

I_{led} = Led current = 20mA

$$R = \frac{V_{cc} - V_{led}}{I_{led}} = 150\Omega$$

The limiting resistor used in the design is 150Ω

3.3.2 Photo detector

A photo detector is usually the most sensitive part of most optoelectronic system hence care should be taken in selecting it. Light dependent resistor was used in this design, it is a photo conductive cell that has two terminals and its terminal resistance is determined by the intensity of incident light falling on its surface.

Photo resistors are commonly available either in cadmium sulphide (cds) form or candium selenide (cdse) form. Resistive photos possess the following advantages

i. High sensitivity (due to large area)

ii. Ease of use (simply light-sensitive resistor)

iii. Low cost

iv. No junction potential

Things that should be considered when choosing photocells are, voltage rating, power dissipation, light source, spectra response of the source and also spectra response of cells.

For the purpose of our design a To-5 with glass top was selected whose voltage rating and power dissipation are 5V and 0.5watts respectively.

Connecting the LDR in a simple voltage divider circuit formed the light dependent voltage circuit as shown below

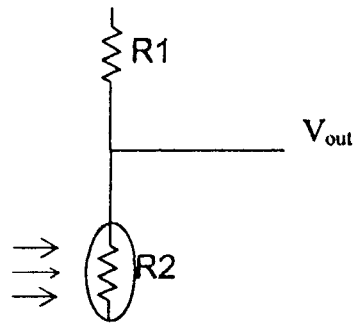


Fig 3.5 Connection of LDR in voltage divider

$$V_{out} = \frac{Vcc \times R_2}{R_1 + R_2} \quad \text{..... (7)}$$

Usually when R_2 is in light, terminal resistance = 1K

When R_2 is in darkness terminal resistance is = 1M

R_1 was chosen to be a 100K variable resistor which is usually preset depending on the illumination of the surrounding environment. Usually an average of 47 is being used

Therefore $R_1 = 47K$

When LDR is in light

$$V_{out} = \frac{\quad \times 1K}{(47+1)K} = 0.104V$$

When LDR is in darkness

$$V_{out} = \frac{5 \times 1M}{(47+1)M} = 4.78V$$

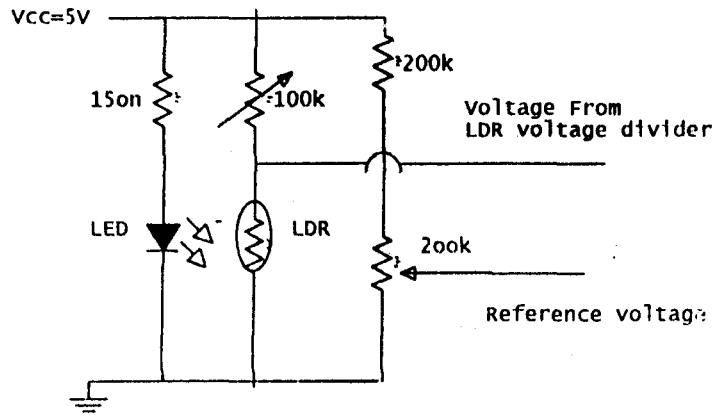


Fig 3.6 Light source and photo detective voltage divider circuit

The circuit shown above is for the arrangement of a single Led and equivalent LDR, this design uses three of such connection to generate three voltage divider that is being fed into the voltage comparating unit, the over all circuit is as shown below.

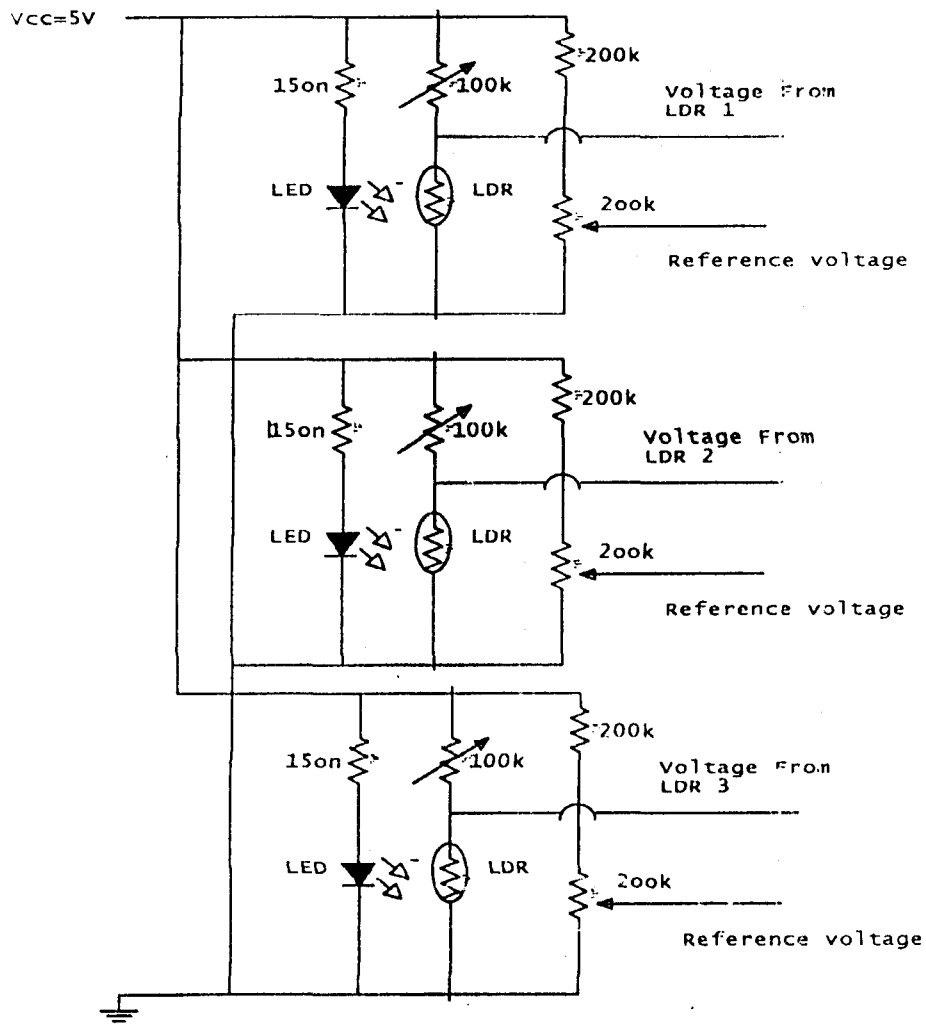


Fig 3.7 Complete connection of LED and equivalent LDR

3.4 Voltage Comparating Unit

A comparator which runs on simple positive supply was considered, the LM339 a quad voltage or current comparator with open collector output was chosen for this design its internal circuitry is as shown below.

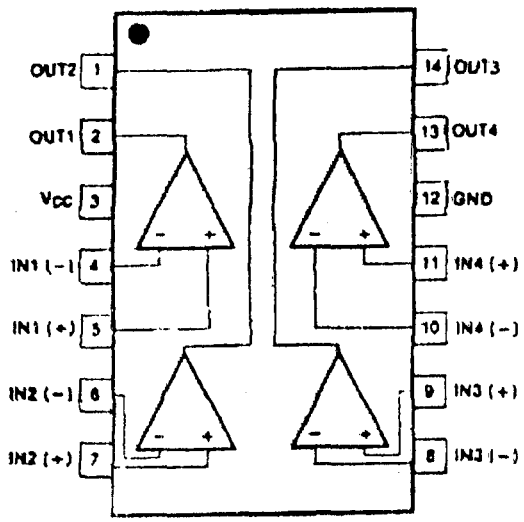


Fig 3.8 LM339 (quad voltage comparator) pin out diagram

It has four independent precision voltage comparators designed specifically to operate from a simple power supply power supply. This design made use of three out of four of the comparators. The three voltage divider connection of LDR are independently connected to the inverting input of the voltage comparator where the non inverting input are being connected to a reference voltage through 200K resistor and a 200K variable resistor.. In this design comparators 1, 3, and 4 was used leaving comparator two unconnected

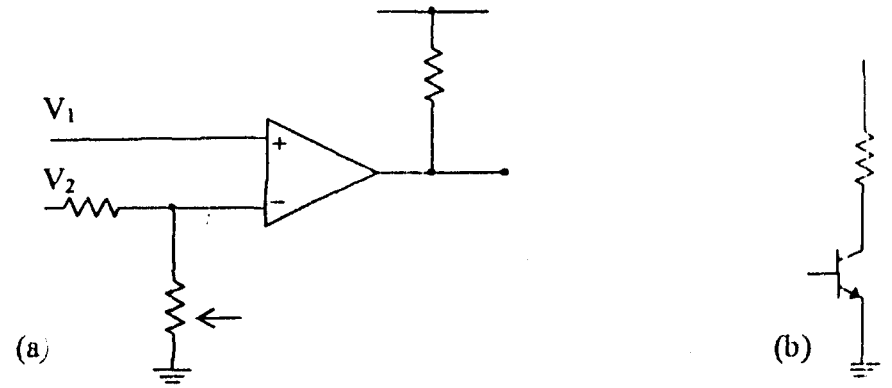


Fig 3.9 (a) comparator with open collector output stage in circuit (b) output stage

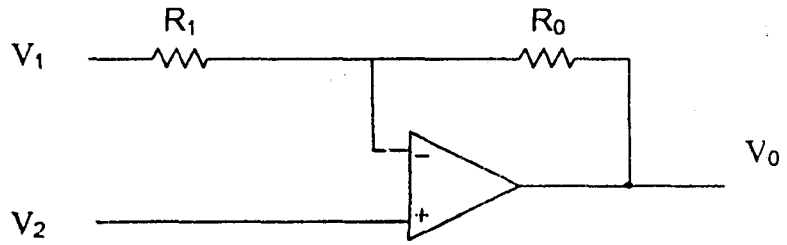


Fig 3.10 connection of amplifier as a summer

Where V_1 = voltage From LDR voltage divider

V_2 = reference voltage

Figure above shows the comparator being connected to function as a summer; this is aimed at providing an out put equal to the difference of the two input signals.

According to super position theorem $V_0 = V_0' + V_0''$

Where V_0' is the output produced by V_1 and V_0'' is that produced by V_2.

From fig we have $V_0' = -\frac{R_0}{R_1} \times V_1$ .....(8)

Also $V_0'' = (1 + \frac{R_0}{R_1}) V_2$ .....(9)

Therefore $V_0 = (1 + \frac{R_0}{R_1}) V_2 - \frac{R_0}{R_1} \times V_1$ ....(10)

Since $R_0 \gg R_1$ then $\frac{R_0}{R_1} \gg 1$

Therefore $V_0 \approx \frac{R_0}{R_1} (V_2 - V_1)$ []

Since from our design $R_0 = R_1 = 47K$,

This implies that $V_0 = (V_2 - V_1)$

When LDR is in light

$V_1 = 0.104V$,

$V_2 = 4.8V$

This implies that

$V_0 = (4.8 - 0.104) = 4.69 \approx V_{cc}$

When LDR is in Darkness

$V_1 = 4.77V$,

$V_2 = 4.8V$

$V_0 = (4.8 - 4.77) = 0.03 \approx 0V$

As seen from the above calculations when $V_{ldr} \geq V_{ref}$ (when in darkness) the comparators output is approximately zero volts. This is because its output stage in an NPN transistor with a grounded emitter and open collector shown in fig 3.9 also when $V_{ldr} < V_{ref}$ (when in light) output transistor is switch off and the output goes to V_{cc}. If a card has not passed through the slot then light beam will be contentiously falling on the Light dependent resistor hence output voltage is maintain at high (logic state of 1).

3.5 **Inverting circuit**

An inverter is an ic that converts whatever comes in its input to the opposite, logically it is called a not gate, this design made use of 7404 which is an hex inverter it has 6 individual note gate connected internally. The pin out is as shown below

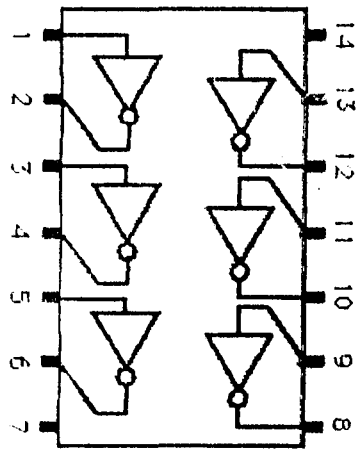


Fig 3.11Pin out of 7404 (Hex inverter)

The inverter can be connected directly to either Cmos, Nmos or Ttl and it has a large operation voltage range, low input current and high noise immunity. Our design made use of the first three inverters and has its input being connected directly to the voltage comparating unit. The truth table below shows the operation of an inverter (not gate)

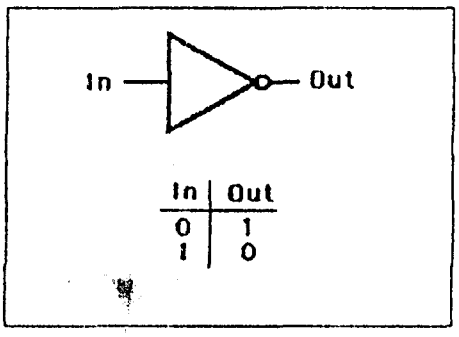


Fig 3.12 Truth table of operation of an inverter

The programme writing into the microcontroller is active high, hence requires a high at any of its three input pins to function, the purpose of 7404 in our design is to providing the required output for the microcontroller for proper functioning. When Ldr is in light output voltage from comparator becomes approximately five volts (logic state 1) this will produce a voltage less than one volts at the out put pin of the inverter (logic state 0). This state keeps the microcontroller in a state of contentiously checking its pin, immediately a card comes to pass it cast a shadow on the ldr thereby putting the ldr into dark. This will cause the output voltage from the comparator to go low, this in turn will produce a high at the output pin of the inverter according to the truth table above, there by causing the microcontroller to then decide.

Table 3.1. Input and Output to LM339 and 7404

State of LDR	Output from comparator (input to inverter)	Output from inverter (input to the microcontroller)	State of Microcontroller
In light (No incoming card)	High	Low	Continue checking pins
In darkness (Incoming card casts a shadow)	Low	High	Make decision

3.6 The decision Circuit

All modern electrical system design today has microcontrollers or microprocessor embedded in it. Microcontrollers are programmable IC which usually comes empty and is

required to be programmable to perform specific task. Our design made use of the Atmel AT80c52, the pin out is as shown below

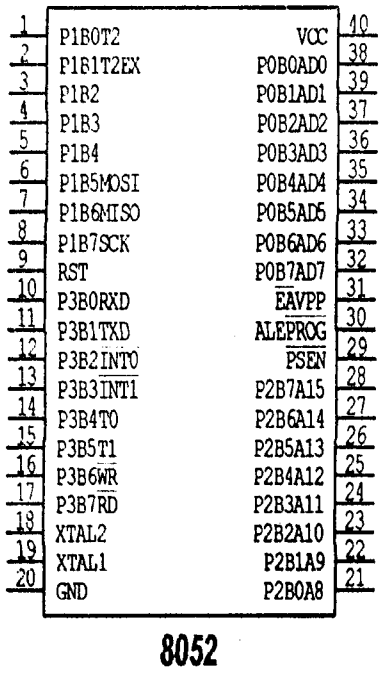


Fig 3.13 Pin output of Atmel AT89C52

The AT89C52 provides the following standard: 8K bytes of flash, 256 bytes of RAM, 32110lines, three 16-bit timer counters, a six-vector two-level interrupt architecture, a full-duplex serial port, on-chip oscillator, and circuitry. In addition, the AT89C52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The idle mode stops the cpu while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The power down mode saves the RAM contents but freezes the oscillator, disabling all other chi function until the next hardware reset.

3.61 **Clock Oscillator**

The clock source unit is made up of two basic components, two 33pf capacitors and one 12MHz crystal. This unit generates the clock pulse for the microcontroller to execute its instruction. The interface between the clock source unit and the microcontroller is shown below.

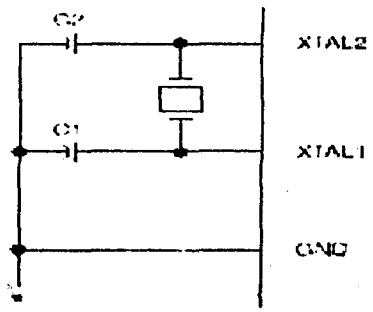


Fig 3.14 Interface between the clock source unit and the microcontroller.

The crystal used is a 12MHz crystal, that is, it will generate 12,000,000 pulses in one second. Normally an 8051 compactable microcontroller executes one instruction in 12 clock pulses. Therefore the microcontroller will be able to perform 12,000,000 divided by 12 instructions in one second. With this fact the time delay was achieved during programming.

3.62 **Making the Decision**

The concept used in the design is that the microcontroller keeps on checking a master pin (pin for total vote), to see if a card is coming. As an incoming card cast shadow on the master LDR, a high is received at pin 1.0 of the microcontroller through the pulse generating circuit. This cause the microcontroller to instruct an increment of

one to the All vote driver. It then goes to check the state of two other pins, the decision taken by the microcontroller is summarized in the truth table below.

Table 3.2 Decision making by the microcontroller

Pin 1.0 (All vote)	Pin 1.1 (LDR A)	P1.2 (LDR B)	Decision Taken
1	X	X	No Decision (keeps on checking)
0	0	0	Clocks P0.3 to increase Invalid v
0	0	1	Clocks P0.1 to increase party A
0	1	0	Clocks P0.3 to increase Party B
0	1	1	Clocks P0.3 to increase Invalid v

Where 0 means Darkness on LDR

1 means Light on LDR

X means don't care condition

As seen from the above truth table when no incoming card, continuous light beam falls on LDR All vote, and the Microcontroller does nothing, immediately a card comes it first casts a shadow on LDR all vote, this causes the microcontroller to count it and makes an increment in the all vote counter unit, after increasing the count the microcontroller then goes to check the state of the other two pins, a state of both Zero and both Ones is considered as invalid vote and thus a clock is sent to increment the invalid vote count. If A is Zero and B is One it means that A is in darkness and B is in light, this will thus, increase the count of A's vote. When A is One and B is Zero meaning A is light and B is in dark, this will course a clock to increase B's vote

Below is a flow chart showing the implementation of the programme

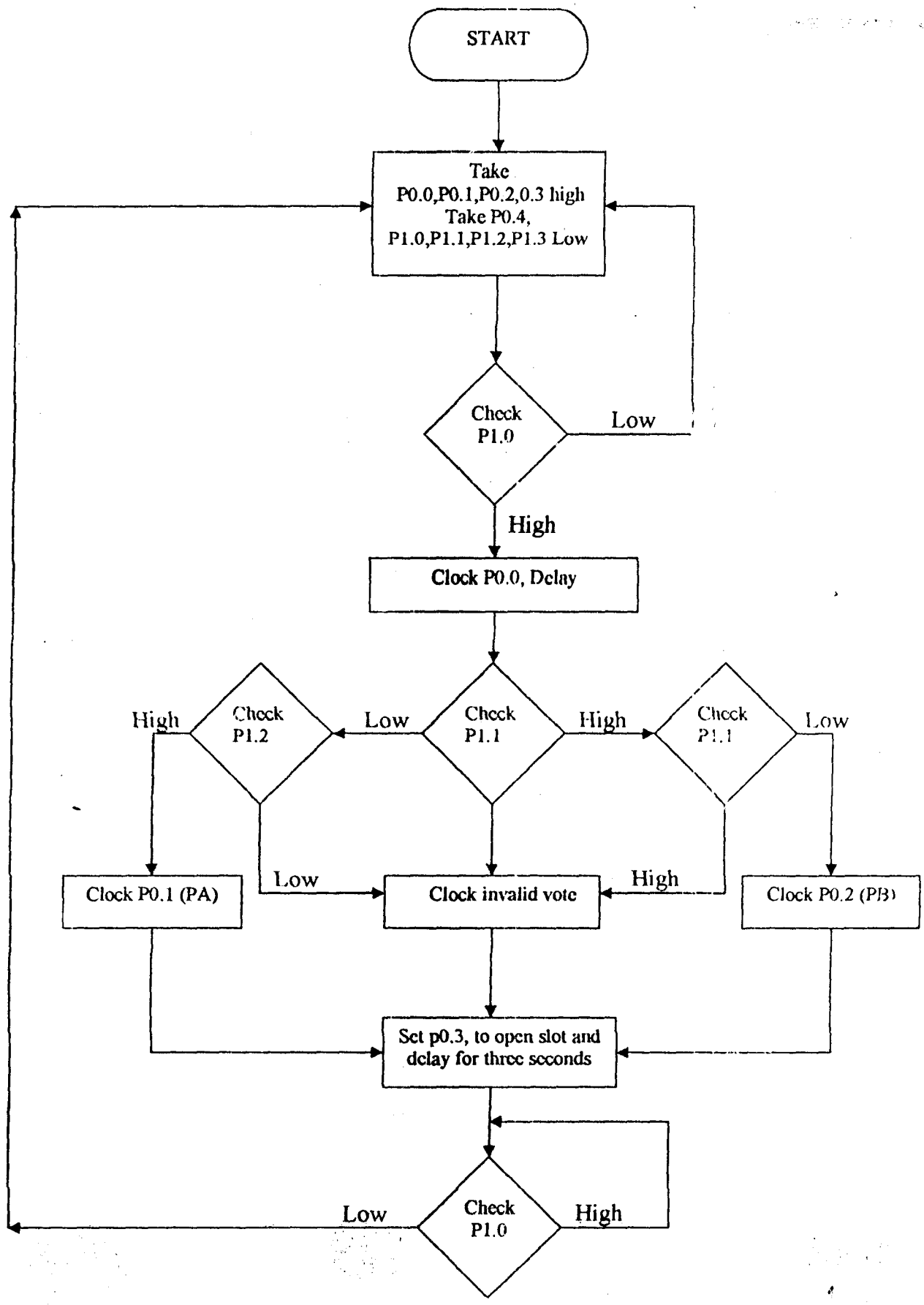


fig 3.15 Flow chart of the programme

3.7 Display drivers and display unit

3.7.1 **Display Drivers**

Display driver is an IC use in this design to communicate between the performing circuit and display unit, several stages is usually executed during driving of a display most especially if it is more than one display. They include Counting, BCD to 7-segment conversion and multiplexing. Our design makes use of a 20 pin microcontroller (AT89C2051), below is the pin out diagram of the AT89C2051

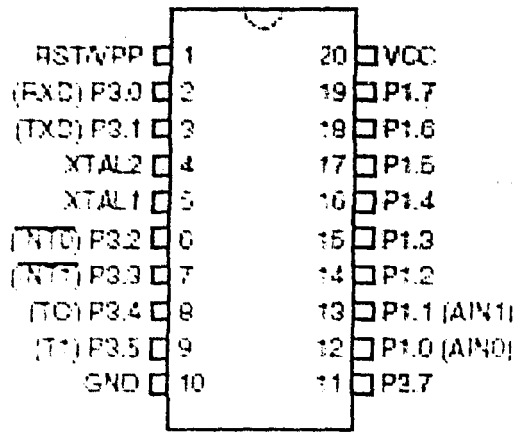


Fig 3.16 Pin out of Atmel AT89C2051

The AT89C2051 is a 20 pin microcontroller which has the following specification: 2K bytes of Flash, 128bytes of RAM, 15 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, a precision analog comparator, on-chip oscillator and clock circuitry. In addition, the AT89C2051 is designed with static logic for operation down to zero frequency and supports two software selectable power saving mod.

It was programmed to be used as a 3 x 7 segment display drivers to count from 1-999. It receives a clock from one pin and increment a count. Stages in the programme include Counting, BCD to 7 segment conversions and multiplexing

3.7.2 **Counting**

Internal of the AT89C51 are registers bank which can hold data, it has four registers bank, each is 8bit wide (1byte), this means maximum value it can hold is 2^8 = 256, we are required to count up to 999 so our design made use of the only user 16bit register which is the data pointer. It is being incremented any time a clock arrived at pin 8 of the microcontroller. The programme also monitors the count so that the count is from 1-999.

3.73 **BCD To Seven segment conversion**

Anytime a clock comes (active low) and an increment is made a segment in the programme is called immediately that converts the value to its equivalent seven segment code. The output is then connected to a 3 x 7 segment to display the number counted. The table below shows the equivalent of a common anode 7 segment display

Table 3.3 BCD to seven segment equivalent (common anode active low)

Display	a	b	c	d	e	f	g	h	Common anode hex equiv.
0	0	0	0	0	0	0	1	1	C0
1	1	0	0	1	1	1	1	1	F9
2	0	0	1	0	0	1	0	1	A4
3	0	0	0	0	1	1	0	1	B0
4	1	0	0	1	1	0	0	1	99
5	0	1	0	0	1	0	0	1	92
6	0	1	0	0	0	0	0	1	82
7	0	0	0	1	1	1	1	1	F8
8	0	0	0	0	0	0	0	1	80
9	0	0	0	0	1	0	0	1	90

3.7.4 Multiplexing

A multiplexer is a device which uses binary address to select which of the input signals appears at the output. Display multiplexing means controlling several displays with one driver. It is done for reason of economy and simplicity, displaying each digit continuously requires separate decoder, drivers and current limiting resistors for each digit as well as separate connection from each resistor, at the end of connection you will have mesh and mesh of wires. Multiplexing is achieved by rapidly switching to each digit in succession at a particular frequency, thus, the persistence of vision makes it appear that the entire display is lit continuously. All common segments in the display are connected together and to appropriate output pin of the driver.

3.7.5 Display unit

Seven segment displays is a common display device which we fine in must digital display electronic. It consist of light emitting diodes (LED) 7 of them arranged in a pattern that can form digits from 0-9 depending on the particular LED which is on at a time. Two type of arrangement present is the common anode and common cathode type. Our design made use of the common anode 7 segment display; this is because a microcontroller sinks current more than it can source. It is an active low display since it requires a logical 0 at its pin to turn on a particular Led. Below is a table that shows the active segment for each decimal digit.

Table 3.4 activated segments for each decimal digit

Digit	Segment activated
0	a,b,c,d,c,f.
1	b,c
2	a,b,d,e,g
3	a,b,c,d,g
4	b,c,f,g
5	a,c,d,f,g
6	a,c,d,e,f,g
7	a,b,c
8	a,b,c,d,e,f,g
9	a,b,c,d,f,g

3.8 **Design Calculation**

For an n-digit multiplexed display the segment current required to produce the same brightness in such a segment would be as if it were individually connected to a port n x I segments. I segment's chosen as 10mA, a digit multiplexed display world require 40mA per segment. This n-fold increase in segment current is to counter the current discontinuity caused by the time slicing due to multiplexing. A 15mA forward current was selected for each segment the required pulsed current therefore is 3 x 15mA = 45mA

The total alphabet used is 7 giving a total current of 7 x 75 mA = 315mA

(7 i.e alphabet a,b,c,d,e,f, and g.)

The transistor used for digit control must therefore be capable of handling this value of pulsed current

Ic = total segment current = 315mA

$$Ic = \beta I_B$$

The 2N2222 transistor has a Hre typically 200

$$I_B = \frac{I_c}{Hre} \quad ; \quad I_B = \frac{0.315}{200} = 1.575mA$$

$$R_B = \frac{Vcc - Vbe - Vol\ (8952)}{I_B}$$

$$R_B = \frac{5 - 0.7 - 0.2}{1.575 \times 10^{-3}} = \frac{4.1}{0.00175} = 2343\Omega$$

A 2.2KΩ base resistance was used to drive current to the base of 2N2222 transistors

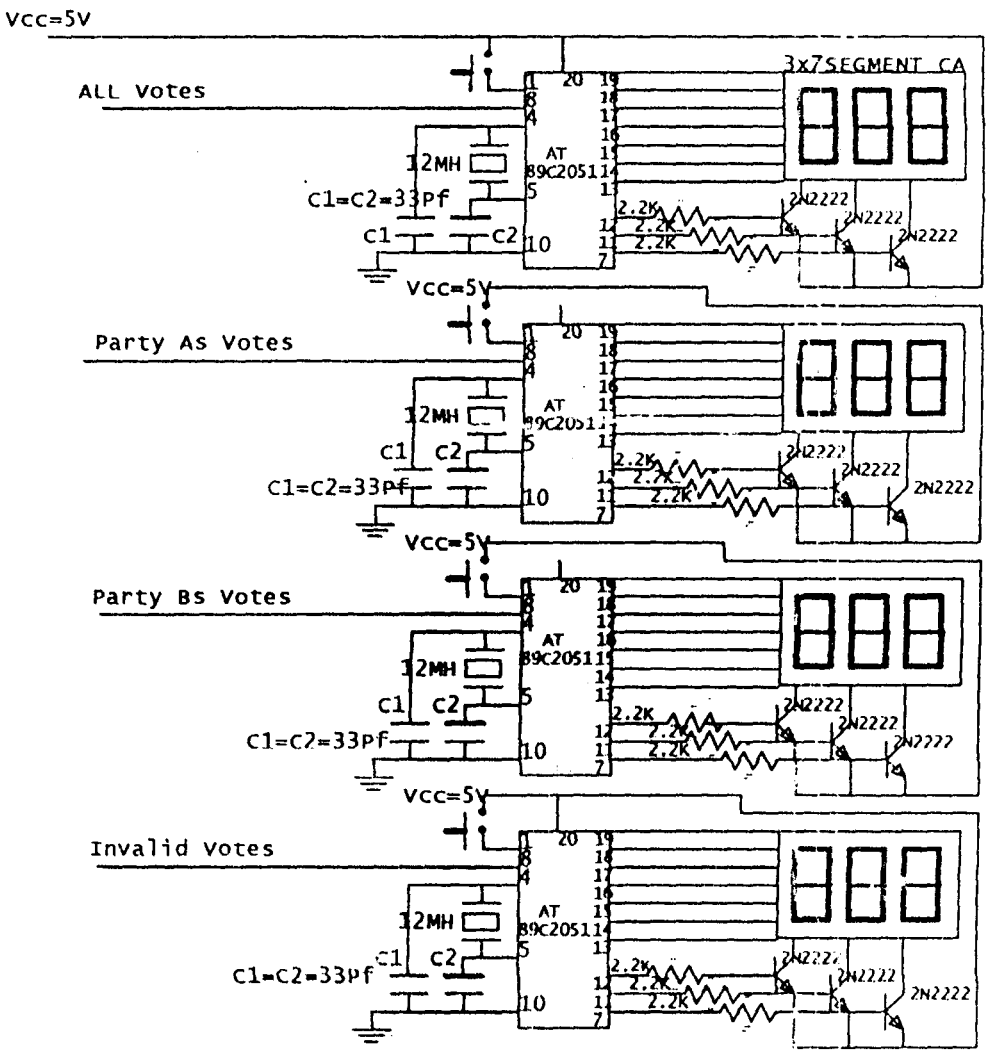


Fig 3.17 Display drivers and display unit

3.9 **Electromagnet**

This is a temporary magnet caused by the passage of current through a coil, it losses its magnetism immediately when the coil is de energized. For the purpose of this design an electromagnet was incorporated with the slot to open up any time a vote is cast so that the card fall off and close up so as to block the slot thus, getting ready to accept an incoming card. The complete circuit diagram is presented in the appendix of this write-up.

Chapter Four

Construction, Testing and Result

4.1 Hardware construction

During hardware construction of the design, the whole system was broken into seven modules for easy construction, testing and trouble shooting. The various modules are

1. Power supply unit.
2. Light source and photo detective unit
3. Voltage comparating unit
4. Inverting unit
5. Decision unit
6. Drivers and display unit
7. Electromagnet unit

4.2.1 Module one: Power supply unit

After getting a good choice of transformer, it is mounted on a Vero board with the primary end (usually the one with thicker wires) connected to Ac supply and the secondary (output) was connected to two ends of a bridge rectifier built with four diode on the Vero board and other two legs have an electrolytic capacitor connected in the right polarity to perform filtering, the positive and negative ends of the capacitors where connected to pin 1, and pin two of the voltage regulator respectively. Led indicator with a series limiting resistor was connected across the outputs of the five volts and six volts output regulator with polarity taken into consideration.

4.2.2 Module two: Light source and photo detective unit

This module comprises the Light source which is also a white colored Led three of them in number in adjacent to three photo resistor, limiting resistor was used to connected the leds, the distance between the Leds and Ldrs where such that it will allow contentious light falling on the Ldr and will also allow a smooth passage of the balot card. The distance between the Ldr and Led was made adjustable.

4.2.3 Module Three: Voltage comparating Unit

This module immediately follows the sensing unit, it contains the comparator quad LM339 which is connected as a summer, three out of four of the comparators where used, this together with the voltage divider circuit of the optoelectronic device causes the sensing depending on the state of the Ldr (either in dark or in light)

4.24 Module Four: Inverting Unit

The output from the voltage comparator was connected directly to a 7404 which is a hex inverter, this was aimed at producing a state to properly drive the microcontroller. Three out of six inverters was made use of.

4.2 5 Module Five: Decision Unit

This consists of the microcontroller and a crystal oscillator to drive it. Out of four, Port one and Port Zero was used with port one as input and port zero as output pins Pins 0, 1, and 2 of port one (I.e P1.0, P1.1, and P1.2) where used respectively to receive the input from the inverter with P1.0 connected to voltage divider of Ldr all, P1.1 and P1.2 connected to voltage divider of ldr A and B respectively. For output Pins 0, 1, 2, 3, 4 of

port zero (i.e P0.0, P0.1, P0.2, P0.3, P0.4) where used to clock all vote, clock party A, Clock Party B, and Set bit for slot to open respectively.

4.2.6 Module six: Drivers and display units

Four output from decision circuit are connected directly to display drivers which drivers 3 x 7segment common anode display. The module consists of a 20 pin microcontroller used as a display driver it uses a crystal oscillator to create pluses to drive it, 2N222 NPN transistors to switch rapidly between each displays and the seven segment displays itself. Connection of this module is on the complete circuit diagram.

4.27 Module Seven: Electromagnet unit

The purpose of an electromagnet in this design is to create a controlled opening, which will open in order to drop a card and close up back to accept another card. It was achieve by winding a coin through and E shaped iron core placed opposed to each other, this E-shaped iron core where place at the bottom of the slot to allow for blockage and opening of the slot as card comes in and dropped into the box respectively.

4.3 Component Layout

The following were observed and done while constructing the hardware:

i. Layout of the arrangement was carefully made so as to get the type of vero board suitable for the construction and that will minimize the use of too much wiring.

ii. The design was built in modules to allow for simplicity and troubleshooting.

iii. Having in mind that excessive heat can damage Ics all Ics sockets where first mounted on Vero board and soldered before inserting the Ic into the socket.

iv. Type of very board used is continuous, so care was taken to detach where continuity is not expected and insulated copper wire where used to connect distance that are not close or are not straight to the lining of the Vero board.]

v. The leads or legs of various components such as capacitors, resistors, leds etc, where reduced so as to prevent short circuit.

4.4 Construction of Casing

The constructed hardware was cased in a box made of aluminum frames with transparent plastic; every where in the box was transparent except the place housing the individual vote count, it was covered with dack plastics to allow for secrecy during voting. Position was made at the top where the card slot will lie; the hardware was inserted in the base of the box. Fig below show the diagram of the constructed box and also the slot.

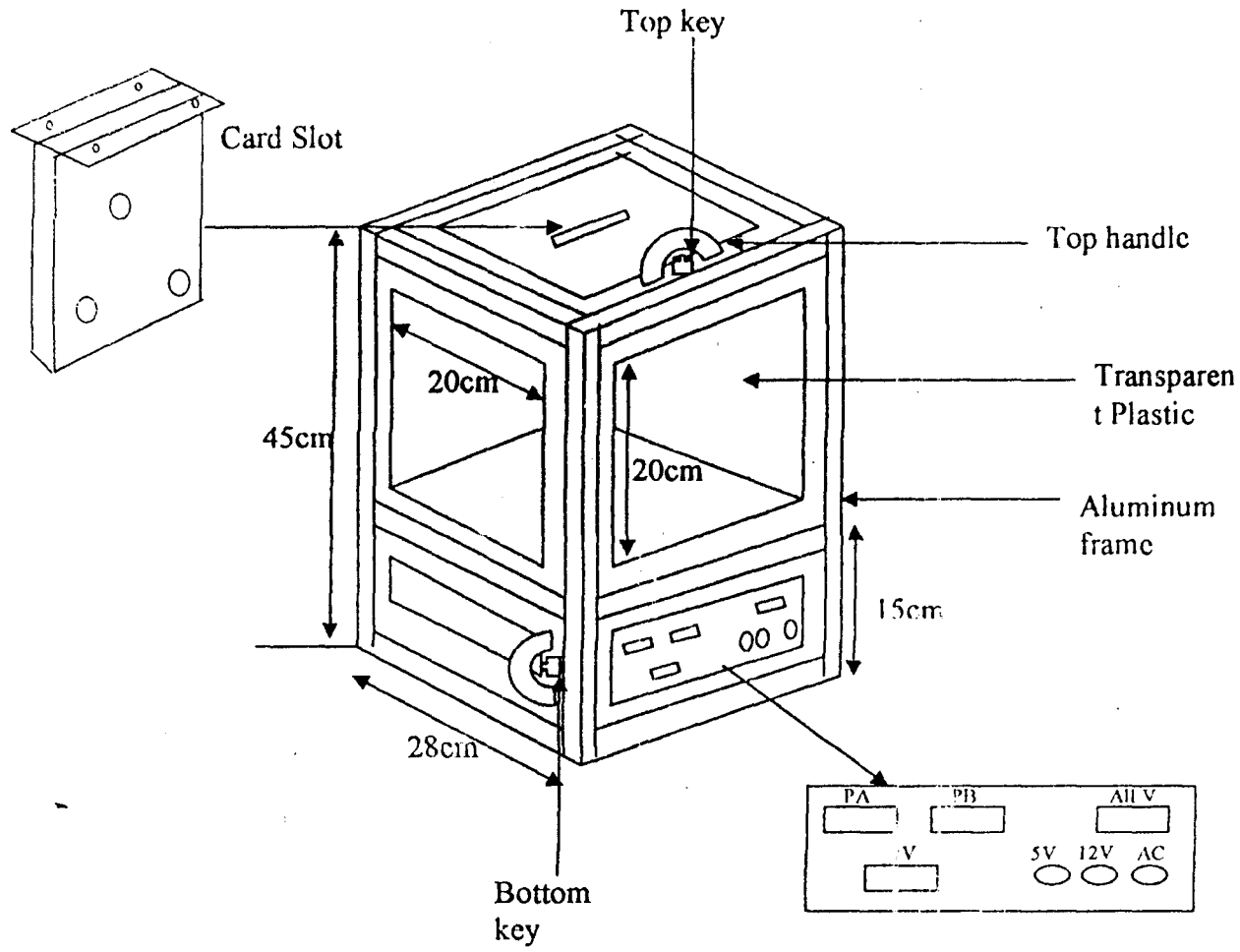


Fig 4.1 Diagram and dimension of box casing used for the project.

4.4.1 **Construction of Slot**

For the construction of the slot light flexible material was used for easy bending to any shape that is required, Aluminium Sheet was used. It was cut to size and with required tools three holes where bore on it and was bent to the desired shape. Since the slot holds the sensing part of the design, it was carefully fabricated having in mind that the Light emitting diodes resides in one side and the corresponding Light dependent resistors on

the other side. Provision was made for adjustment of the slot size(distance between adjacent aluminium plates) to allow for freely movement of ballot card The boare hols on aluminium are as shown below.

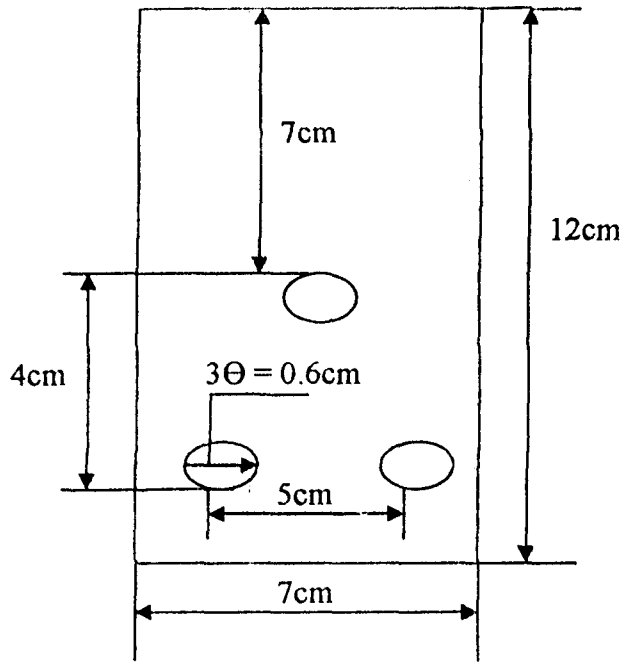


Fig 4.2 Dimension of holes on aluminium plate

4.5 Testing

Testing of the construction was carried out module by module before the final over all tests was done. A light emitting diode was used at different stages to monitor the behavior of the system, after ascertaining that the clock pulse for the four displays was received depending on the perforation on the incoming card, the construction was then coupled together.

4.6 **Result and discussion.**

Voting card was constructed and used in testing; it was observed that with the front side of the card facing you a perforation on the left side of the card causes an increase in total by one and also the display for Party As vote also increases by one. With a perforation on the right side of the card a unary increase in total vote with an increase in party B's vote was observed. An increment in invalid vote was noticed when no perforation on the card and also when both side were perforated. The table below summarizes the result obtain

Hole on Card	All vote Display	Party A's Display	Party B's Display	Invalid Vote Display
On the Left	Increases by one	Increases by one	No increment	No increment
On the Right	Increases by one	No increment	Increases by one	No increment
No Hole	Increases by one	No increment	No increment	Increases by one
Both Perforated	Increases by one	No increment	No increment	Increases by one

Table 4.1 Test result obtained

The card was built with the perforation on the left labeled party A, while that on the right was labeled party B, to vote for party A you simply pill off party A on the card to make a hole there this will cause an increment in party A's vote when the card in inserted in the slot, to vote for party B you simply pill off party B off from the card and you vote will be counted for party B. No hole or both holes on card makes the card an invalid vote. At the end of the test it was observed that

Total vote = Party A's vote + Party B's vote + Invalid Vote

The dimension of the card is as shown below

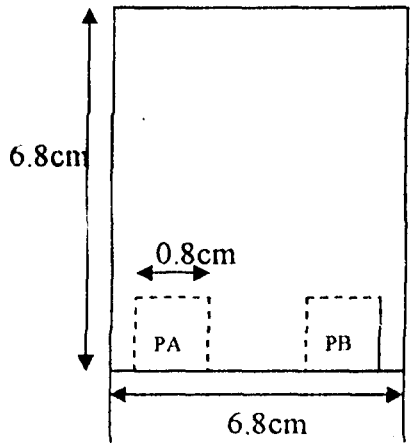


Fig Dimension of peforated Ballot Card

CHAPTER FIVE

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusion

The aim of this project was to construct a voting box which will present an easy, effective, efficient and transparent electoral process in which at the end of the construction was achieved. The design made use of low operating voltage and low power consumption which is a great advantage in modern electronic design, an aluminium was chosen for the casing which makes the casing light and cheap.

5.3 Problems Encountered

The following problems and difficulties were encountered during thee design and construction

1. purchasing of ICs
2. Due to high precision in control of the slot (i.e automatically opening to drop a card and automatically closing up to block a card) we encounter problems with it.
3. Due to its complexity of the circuit it was hard troubleshooting.
4. No device to test ICs to ascertain its functionality.

5.4 Recommendation

i. School should provide a means for easy access of electrical component so as to ease the student the stress of traveling to obtain Ic, and also to get it at a cheaper price.

ii. For any one who intends to improve on this project, more examination and calculation should be done for the control of the slot in order to obtain an electromagnet automatically operated slot.

iii. A liquid crystal display can be incorporated in the display unit for a better display of the output result

iv. Sensing device with higher sensitivity can be incorporated in the design to make for high precision in reading of the card.

v. Modification can also be made in the design for the box to be able to differentiate punched ballot papers for more than two political parties.

vi. This design can be modified to be interfaced with the internet so that after the entire voting process the result can simply be submitted to the internet for easy collection of result and prompt announcement of result

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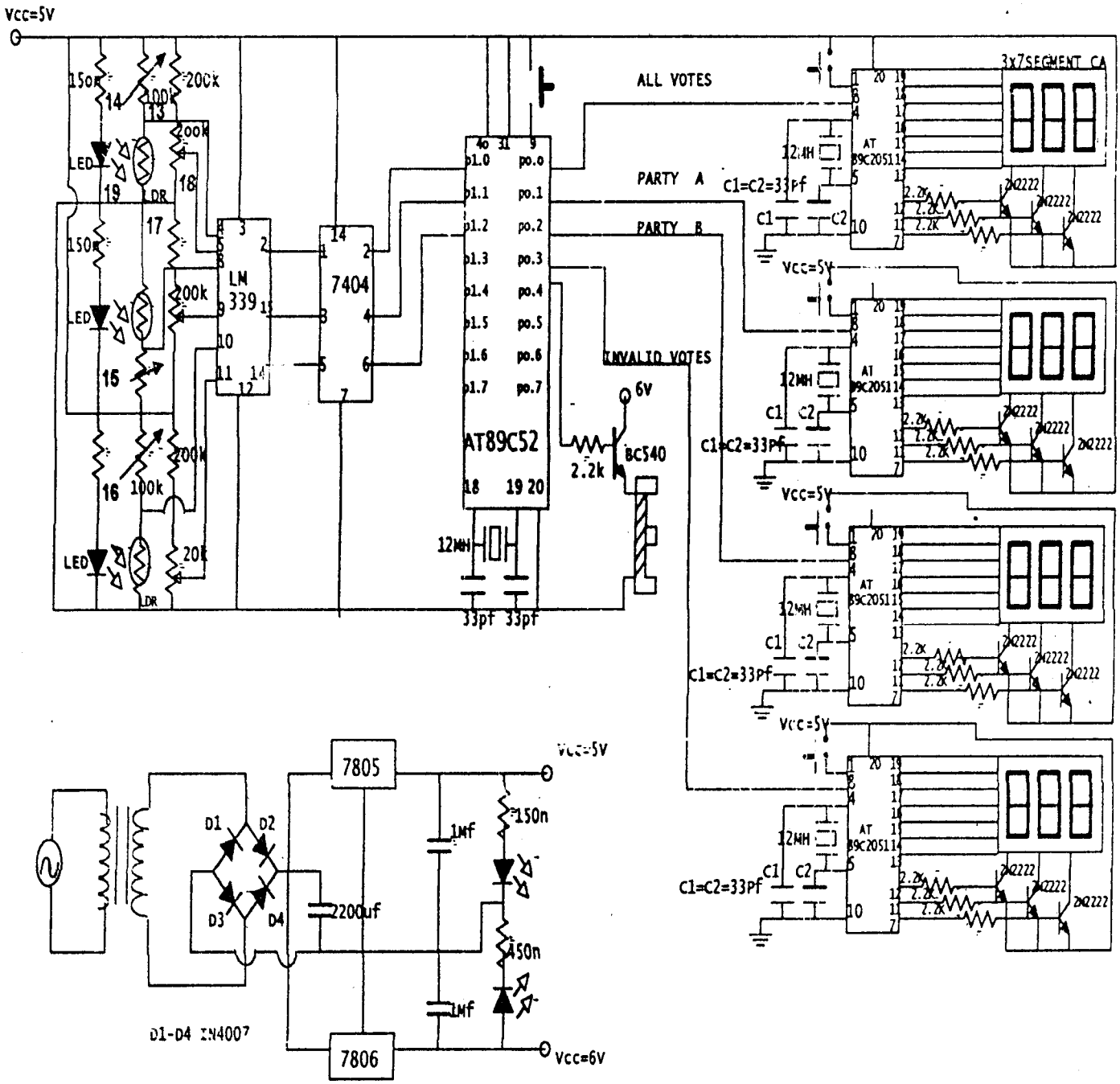
Appendix

Complete Circuit Diagram of the Design



Programme of the Decision Circuit

```
        ALL EQU P1.0
        PA EQU P1.1
        PB EQU P1.2
        CLOCKALL EQU P0.0
        CLOCKA EQU P0.1
        CLOCKB EQU P0.2
        SLOT EQU P0.4
        ALARM EQU P0.5
        CLOCKIV EQU P0.3

MAIN:
        CLR ALARM
        CLR ALL
        CLR PA
        CLRPB
        SETB CLOCKALL
        SETB CLOCKA
        SETB CLOCKB
        SETB CLOCKIV
        CLR SLOT
        JB ALL, CHECK-STATE
        SJMP MAIN
CHECK-STATE
        CLR CLOCKALL
        LCALL DELY-ONEFOUR-SEC
        SETB CLOCKALL
        LCAAL DELAY-ONE-SEC
        LCALL DELAY-HALF-SEC
        JB PA, CHECK-SECOND-PINA
        JNB PA, CHECK-SECOND-PINB
 CHECK-SECOND-PINA
        JB PB, INVALID-VOTE
        JNB PB, VOTE-PARTYA
 CHECK-SECOND-PINB
        JB PB, VOTE-PARTYB
        JNB PB, INVALID VOTE
  VOTE-PARTYA:
        CLR CLOCKA
        LCALL DELAY-ONEFOUR-SEC
        SETB CLOCKA
        SETB SLOT
        LCALL DELAY-TWO-SEC
```

```
            LCALL DELY-ONE-SEC
            CLR SLOT
            SJMP STAY1
SONUD1: SETB ALARM
STAY1:  JB ALL, SOUND1
            LJMP MAN
VOTE_PARTYB:
            CLR CLOCKB
            LCALL DELAY_ONEFOUR_SEC
            SETB CLOCKB
            SETB SLOT
            LCALL DELAY_TWO_SEC
            LCALL DELAY_ONE _SEC
            CLR SLOT
            SJMP STAY2
SOUND2: SETB ALARM
STAY2:  JB ALL, SOUND2
            LJMP MAIN
INVALID_VOTE:
            CLR CLOCKIV
            LCALL DELAY_ONEFOUR_SEC
            SETB CLOCKIV
            SETB SLOT
            LCALL DELAY_TWO_SEC
            LCALL DELAY_ONE_SEC
            CLR SLOT
            SJMP STAY3
SOUND3: SETB ALARM
STAY3:  JB ALL, SOUND3
            LJMP MAIN
DELAY_ONE_MILLI:
            MOV R2, #250
LOOP_MILLI:
            NOP
            NOP
            DJNZ R2, LOOP_MILLI
            RET
DELAY_ONEFOUR_SEC:
            MOV R3, #250,
LOOP_ONEFOUR_SEC:
            LCALL DELAY_ONEMILLI
            DJNZ R3, LOOP_ONEFOUR_SEC
            RET
DELAY_HALF_SEC:
            LCALL DELAY_ONEFOUR_SEC
            LCALL DELAY_ONEFOUR_SEC
```

```
        RET
DELAY_ONE_SEC:
        LCALL DELAY_HALF_SEC
        LCALL DELAY_HALF_SEC
        RET
DELAY_TWO_SEC:
        LCALL DELAY_ONE_SEC
        LCALL DELAY_ONE_SEC
        RET
        END
```