DESIGN AND CONSTRUCTION OF A DC POWER PACK WITH A DIGITAL READOUT

BY

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(2003/14844EE)

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A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE BACHELOR OF ENGINEERING DEGREE IN THE DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
FEDERAL UNIVERSITY OF TECNOLOGY, MINNA, NIGER STATE.

NOVEMBER, 2008.

ATTESTATION/DECLARATION

I ONYEMA C. OBINNA declare that this work was done by me and has never been presented elsewhere for the award of a degree. I also hereby relinquish the copyright to the Federal University of Technology, Minna.

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ENGR. DR. Y.A. ADEDIRAN .	.....
(Name of H.O.D)	(Name of External Examiner)
.....	.....
(Signature and date)	(Signature and date)

DEDICATION

I hereby dedicate this project to my Lord and Saviour, Jesus Christ, to my wonderful parents Engr. N.I Onyema and Mrs. Grace Onyema, my beloved brothers and sisters and friends.

ACKNOWLEDGEMENT

All glory and adoration belongs to the creator of the world. Without him, this project would have been a mirage. A sublime tradition says, he who is ungrateful to God, will be ungrateful to man.

I wish to commend all the lecturers of the Electrical and Computer Engineering Department, the H.O.D, Engr. Y.A Adediran, the project Coordinator, Dr. E.N. Onwuka, my supervisor, Mr.Suleiman Zubair, for your support and immense encouragement. You encouraged me to strive for excellence, for that I am sincerely grateful.

To my father, Engr. N.I Onyema , for standing by me and believing in me. My mother, Mrs. Grace Onyema ,for your prayers for me and all the love you showered me,I say thank you. To my mum ,Mrs. Grace Onyema,I love you.and to my siblings, Joy, Ozichi, Uzoma, Eze, Stella, and Enyioma,you guys are the best, my friends,J. Amadi ,Peter,Amadi,JonathanAwadi, Yinka, Deji, Michael, Walezi, Eraser, you all made my stay in school an educative and refreshing experience.

Finally, to my caring and loving colleagues not mentioned, I say a big thank you to you all and may you be rewarded in folds.

ABSTRACT

This project presents the design and construction of a DC power pack with a digital readout.The project incorporates all the important features of an ideal power supply system for powering up all electronic devices within 5V. This project is durable, efficient minimal cost to the consumer.The whole system is designed around microcontroller. This constitutes the whole system unit of an ideal DC power pack with a digital readout.

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CHAPTER ONE

GENERAL INTRODUCTION

1.0 INTRODUCTION

Engineering is all about making life easier through the application of science for the designing and building of machines and structures. In a bid to do this, various researches are being carried out to understand the phenomenon around us. Everyday research is being made to try and maximize the earth` s resources and potential. Electrical engineers strive to find other alternative means of power supply. One of the fields which has experienced a lot of the research is the area of dc power pack and it usefulness to man. This research looks at how a step-down transformer pulse rectifier can be used for power generation and for the general good of mankind.

This project involves a dc power pack with digital readout mainly for powering electronic devices such as mp3 players, cell phones, PDA`S e .t. c. Its design is simple and economical. Its application is targeted towards areas where electricity supply is minimal and epileptic.DC power pack with digital readout usage , has dramatically increased over the last few years due to devices such as cell phones,mp3 players, PDA`S e. t. c. Consumers must constantly power these devices at home to obtain just a few hour of working functionality . I mean to design a power pack that would enable consumer to charge up virtually all the small electronic devices via dc power pack. This project is advantageous to both the consumer and the environment. I choose this project because I saw the need in the market for an alternative powering device that can power a wide range of electronic devices and circuits, it will

incorporate both our specialities in electrical engineering power and circuitry.

1.1 AIMS AND OBJECTIVES

The aim of this project is the design and construction of a dc power pack with a digital readout that will power electronic devices when voltage supply is low and enable a readout of the status of the load applied. The design is aimed at simplicity,stability, reliability and flexibility for efficient and stable power supply .It is also an attempt to show the immense potential on how dc power pack can be achieved.

BENEFITS:

i. The load status will be displayed for the user

ii. Ensures that the intended powering of any electronic device within 5V is powered

iii. It is cheap and therefore affordable.

iv. Users will continously power there electronic devices irrespective of the nature of power supply from PHCN.

1.2 METHODOLOGY

1.2.1 CONCEPTUALIZATION

This is the stage in which the project was conceived. Firstly, the consideration of the problem of getting all the electronic devices below 5volts charged up when ever there is epletic power supply. The next was considering the most effective and economic means of solving this problem. The challenges that would be faced were also considered at this stage.

1.2.2 CONSULTATION

This involves seeking expertise advice about what the project entails in terms of cost and time. Advice was sought from staff of the institution, fellow students with technical know-how , about how the project could be achieved.

1.2.3 ECONOMIC CONSIDERATION

At this point, the amount of money that would be spent on the project was considered. A fixed amount was set aside for the project. This was done to avoid financial constraints during the construction stage of the project .A market survey was carried out to check the prices of the required components and find out where these components could be gotten at reasonable prices.

1.2.4 RESEARCH AND DESIGN

This involved checking on scientific materials and books on how to commence the project. Relevant websites with useful information about the designs, constructions and implementation of dc power pack devices where also visited. The aim was to get the most effective and economically viable design for the project. This stage involves the simulation of the circuit design on an electronic software application, electronic workbench.

1.2.5 CONSTRUCTION

This is the actual fabrication. Here, the circuit was first tested on a breadboard before transfers could be made to the vero-board. This stage involved component testing, soldering and the packaging of the project design.

1.3 SCOPE OF THE PROJECT

- This project focuses on the construction of a dc power pack with a digital readout. It supports the use of a step down transformer plus a rectifier to the dc supply and rectify to the desired dc output voltage, which is about 5V for supply. It employs the use of an analog to digital converter and a microcontroller that will enable the display of the load status which is in volts.

CHAPTER TWO

LITERATURE REVIEW

2.1 History and Development of Power supplies

All the power supplies provide electrical energy to do work; but now this feat has been accomplished over the countries has varied considerably.

The first power supply was invented in 1745, was called "the LEYDENJAR", it could store large electric charges created by electrostatic devices such as electrophorus. The charge could be drawn from the jar and put to work (1).

In 1800, Volta created the first battery, "the VOLTAIC PILE". This quite reliable source of power than produced electricity by means of a chemical reaction. This invention was a stepping stone for the subsequent manufacture of direct current cell and batteries.

Thomas Edisson's invention of the incandescent light bulb in 1879 has created a demand for electricity, so he established a DC-generated power supply company in New York City (1). Direct current supplies has two main disadvantages: power production was limited by arcing the brushes that drew electricity from the dynamos's rotor and long distance transmission was prevented by resistance.

The use of Zener diode to produce a regaulated DC voltage supply regardless of fluctuation in supply and the current draw, by the load. Much later, transistors were included in the designs to improve regulation. Rectifier IC's later replaced the bridge rectifier arrangement o discrete diode components.

DC power pack has been in existence since 15-20 years. In the past, most power packs are without a digital readout in order to display the charging status of the battery and also without an incorporated microcontroller to aid the display.

DC power pack has been in existence since 15-20 years. In the past, most power packs are without a digital readout in order to display the load status of the battery and also without an incorporated microcontroller to aid the display.

In recent times, some works have been carried out on DC power pack with digital display incorporated such as Duracell (R) power pack 600HD portable power, power pack stabilizer with digit display, which provides the user with information on the status of the unit.

2.2 LIMITATIONS OF PAST WORKS ON POWER PACK

1. The load status were not indicated or provided for users .
2. Components used in realizing it were fading and outdated, compare to recent works e.g micro controller which is cheaper in terms of cost.
3. There was no provision of protection of battery from user error.

2.3 BRIEF SCOPE ON RECENT WORKS POWER PACK

Recent works have been able to actualize the past work limitation by incorporating some modern features in order to make life easier for users.

Some components used are transformer, rectifier, micro-controller etc.

2.1.1 Transformer is an electrical device that transfers energy from one electrical circuit to another by magnetic coupling without moving parts. It is often used to convert between a high and low voltage and accordingly between low and high current.

Transformer is an important element in the development of high-voltage power transmission and central generating station etc.

There are two types of transformer, step-up and step-down transformer. In order to actualize this project, a step down transformer is needed in order to reduce the D.C supply.

1874, Braun noticed that this was a natural effect on some crystals particularly galena. Crystal rectifier gave growth to crystal radios and eventually to the development of the transistor.

Three types of rectifier circuits are used for single phase rectification. There are-:

2 Half wave.

3 Full wave

4 Bridge full wave rectification.

In the half-wave rectifier, a single diode conducts only on one half cycles, though a single circuit, it has the main disadvantage of low efficiency which cannot be greater than 50%.

5 The full-wave rectifier has two diodes each conducting on alternating half cycles to give much high efficiency. However, to achieve this, a transformer with a centre tapped secondary winding is necessary. This means that the number of turns is required on the secondary winding. This circuit was common when valve rectifiers were transformers than to use more valves.

6 The full-bridge wave form rectifier, now the circuit of choice uses four diodes to achieve rectification over the whole cycle.

2.1.3 MICROCONTROLLER

Since 1975, Intel has been producing many different types of Micro controllers. In general, each microcontroller that Intel has made falls into one of the families below. The families differ mostly in instruction sets and architecture. Within each family, there are different CPUs while each CPU may have the same core; the feature set can vary a lot. Common differences within a single family are:

1 On-Board ROM size

2 On-Board RAM size

3 Re-programmability

4 ADCs

5 Timers

6 And many other features.

Micro controller usually contain the programs, they run on the chip themselves, or off the chip on a ROM. Intel used several conventions to specify weather the chip had ROM or not and weather it was programmable.

1 80xxx ROMLESS

2 86xxx UVEP ROM

3 82xxx Are designed mask ROM (8242 keyboard controller).

4 83xxx Mask ROM

5 87xxx OTP ROM

Intel introduced MCS-41 in 1979, MCS-51 in 1980, MCS-96 in 1982 etc. The purpose of this, was to realize the desired output within a short frame of time [3] .

The essence of this product is to design a de power pack with a digital readout incorporated.

3.1 DC POWER SUPPLY

A 24V 1A step down transformer is used to provide the primary voltage input into the adjustable regulator sub system .The transformer is converted to a four diode full wave rectifier as depicted in fig 3.1The 24V AC voltage is transformed into pulsating dc voltage of peak amplitude :

$$V_{dc} = [V\ r\ m\ s\ \sqrt{2} - 1.4] \text{ volts} \quad \ldots\ldots(1)$$

For a 24V r m s secondary voltage,

$$V_{dc} = [\,24\ \sqrt{2} - 1.4\,] \approx 33V \quad \ldots\ldots(2)$$

This value of voltage is rectified by a capacitance of value deduced from the expression;

$$C = \frac{it}{v} \quad \ldots\ldots(3)$$

I = maximum Load current

$$t = \frac{1}{2} F\ [FWBR] \quad \ldots\ldots(4)$$

F = 50 HZ main frequency

V = maximum allowable AC ripple voltage.

The maximum AC ripple voltage is tired at 2Vand the maximum load current is made equal to the transformer current rating [1A].

C is thus, calculated as shown below,

$$C = \frac{(1 \times 1/2 \times 50)}{2} \text{Farad} = \frac{1 \times 0.01}{2} = 0.005F = 5000\mu F \quad \ldots\ldots(5)$$

A value of 4700μF with a cook up voltage of 35V dc is selected for use.

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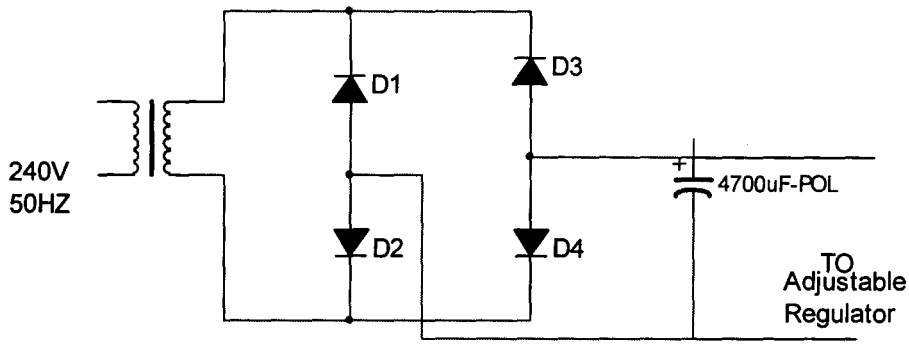

Fig 3.1 30V dc system power supply

A 5V auxiliary dc supply is gotten from the 30V dc input. This is realized as shown below,

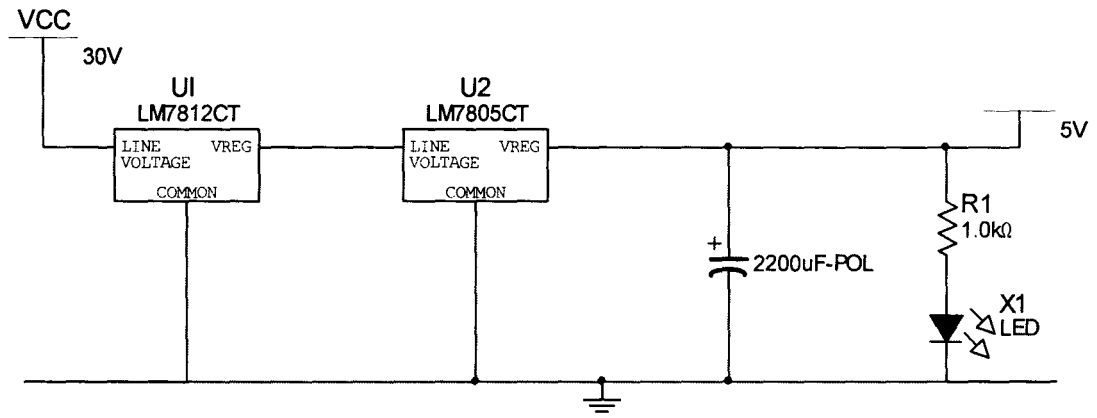

Fig 3.2 +5v system dc logic supply

A 7805 5V regulator is used to produce the required 5V system voltage from the 12V output of a 7812.The 5V dc is stabilized by a 16V 22μF capacitance and fed to the digital portion of the system. A power _on LED indicator is used for indicating connection to local main AC .The LED is operated off the 5V dc supply via a current limiting resistance value deduced from;

$$V_{LED} \cong 1.7V$$

$$I_{LED} = 5mA \sim 20mA$$

A norminl LED continous forward current of 10mA chosen ,

3.2 ADJUSTABLE VOLTAGE REGULATOR

To meet the intended design objectives, an adjustable voltage regulator sub system is incorporated in the system realization .An integrated circuit (IC) 3- terminal dc voltage regulator is used. An LM317Y regulator with the following specifications: Insert LM317Y datasheet here is used .The is configured for regulator operation as depicted in fig 3.3 below,

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} \quad \text{.....(11)}$$

$$\frac{5 - 0.7}{0.01} = 0.0024$$

$$= 4.3 / 0.0024$$

$$= 1.8k\Omega$$

A value of 1kΩ is used for Rb and the on- time of each digit is kept at 1ms.

3.6 SOFTWARE OVERVIEW

The system control software is modularized for easy debugging and easy understanding .The control software consists essentially of the following modules;

1. System initialization
2. control conversion modules.
3. DC voltage computation module
4. Display update module

The software listing is given in the appendix.

3.7 SYSTEM INITIALIZATION ENTRIES

The entries are excited immediately. The system comes out of reset , this routine initializes the system resources and user defined variables relevant to design objectives.

3.5.1 ADC CONTROL CONVERSION MODULE

This module controls the Analog to Digital conversion process.

3.5.2 DC VOLTAGE COMPUTATION MODULE

As a result of the attenuation provided at the ADC output and the 5v full scale reference voltage, software computation is used to recover the value of the initial DC voltage prior to attenuation.

For a 5v FS input voltage, an input – output relationship of

$$5v = 255$$

$$Xv = y \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (12)$$

$$5y = 255x$$

$$\frac{Y}{X} = \frac{255}{5}$$

$$\frac{Y}{x} = 51\ 5 \qquad ; x = \frac{y}{51}$$

Vhere y = binary output value of the ADC

X = corresponding input voltage on pin 6 producing an output of y.

overcome the ± 6 input attenuation, the (y / x) is multiplied by 6 to obtain the original voltage present on the LM317T output before attenuation.

)ISPLAY UPDATE MODULE

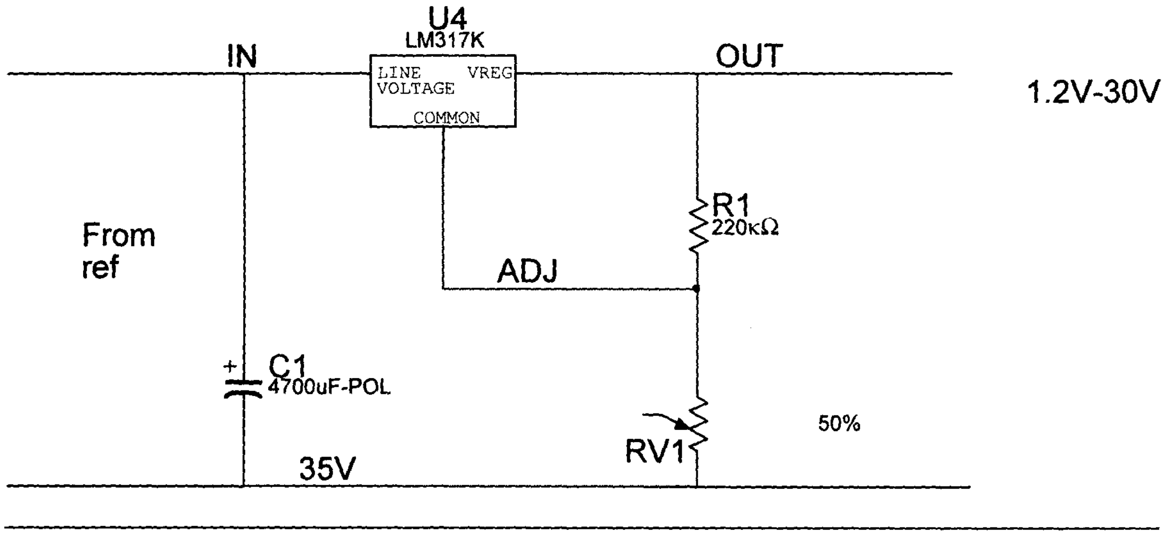

Fig 3.3 Adjustable voltage regulator

This has an output voltage deferred try the values of Rv1 and R I , from the equation below,

$$V_{out} = \left[1.25 \left(1 + \frac{RV1}{R1}\right)\right] \text{ volts} \qquad (6)$$

1.25 = internal reference voltage

RV1 = Resistance between the adjustable pin and ground

R1 = Resistance between the output and adjust pin (typically 220Ω)

The device has a maximum input voltage of about 37V and a rated output current of 1.5A at low input - output differential voltages.Rv1 resistance is adjustable in order to produce the desired output dc voltage as determined by the expression for V out.

3.3 8- BIT ADC SUB SYSTEM

Since part of the design realization is to provide a visual indication of the output voltage , a means of converting the dc output voltage to analog to digital value required. Thus , an analog to digital converter is required.

Since speed and regulation requirement were easily met by anADC0804 ADC, the device is detected as the interface between the controller and the voltage regulator sub system .The ADC 0804 has the specifications stated below;

Insert ADC 0804 datasheet here .The device is interfaced with the system controller over the byte- wire p1.Converter control logic is generated using p3.0, p3.1, and p3.2 .These pins are designated as chip select , adc write , and adc_intl respectively .The ADC is setup for operation with a full scale voltage of 5V , i.e. a 5V input dc voltage on pin 6 produces the code ffh to appear at the output .The converter is run off a clock source determined by the values of RC components connected to pin 19 and 4 as shown below.

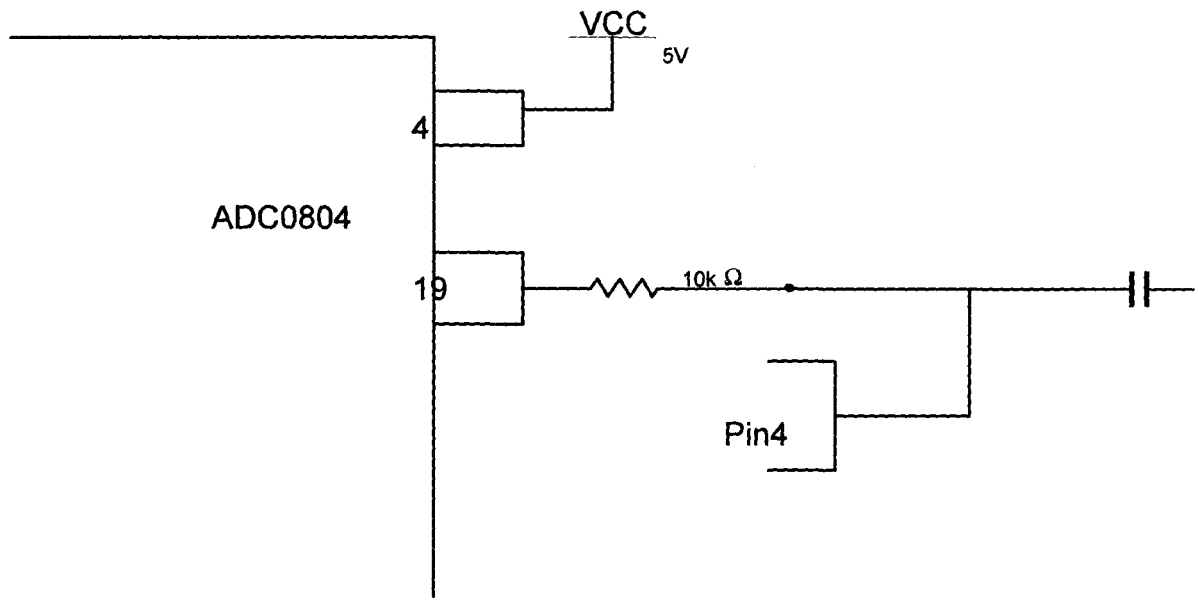

Fig 3.4 ADC clock source

The device supports a minimum clock of 1000 KHZ and an upper limit of 1.46MHZ .A value lying between these two is selected.

$$F = \frac{1}{1.1\,RC} \quad \ldots\ldots (7)$$

R = Typically 10kΩ

C = 150pF

$$F = \frac{1}{1.1 \times 10^{4} \times 150 \times 10^{-12}}$$

$$= 8.760 \times 10^{-11}\text{kHZ}$$

Conversion is initiated by taking CS low, then pulsing WR low , and then high .WR is bracketed by CS going high again.The typical conversion time of 100μs of the ADC0804 is

taken into account in the software as the adc_ intl pin functionality is not used should the device fail for any reason.

Since the maximum input into the ADC is 5V , a potential divider is needed at the input to reduce the adjustable input voltage within the specified limits.

A maximum regulated output voltage of 30V is designed for using a 12-0-12V transformer .At 30V dc output voltage , the display should display 30.0 and the dc voltage into the ADC is divided down by six (6) such that at 30V input dc , the input into the regulator is 5 , corresponding regulator is 5 , corresponding to 255_{10} output word.

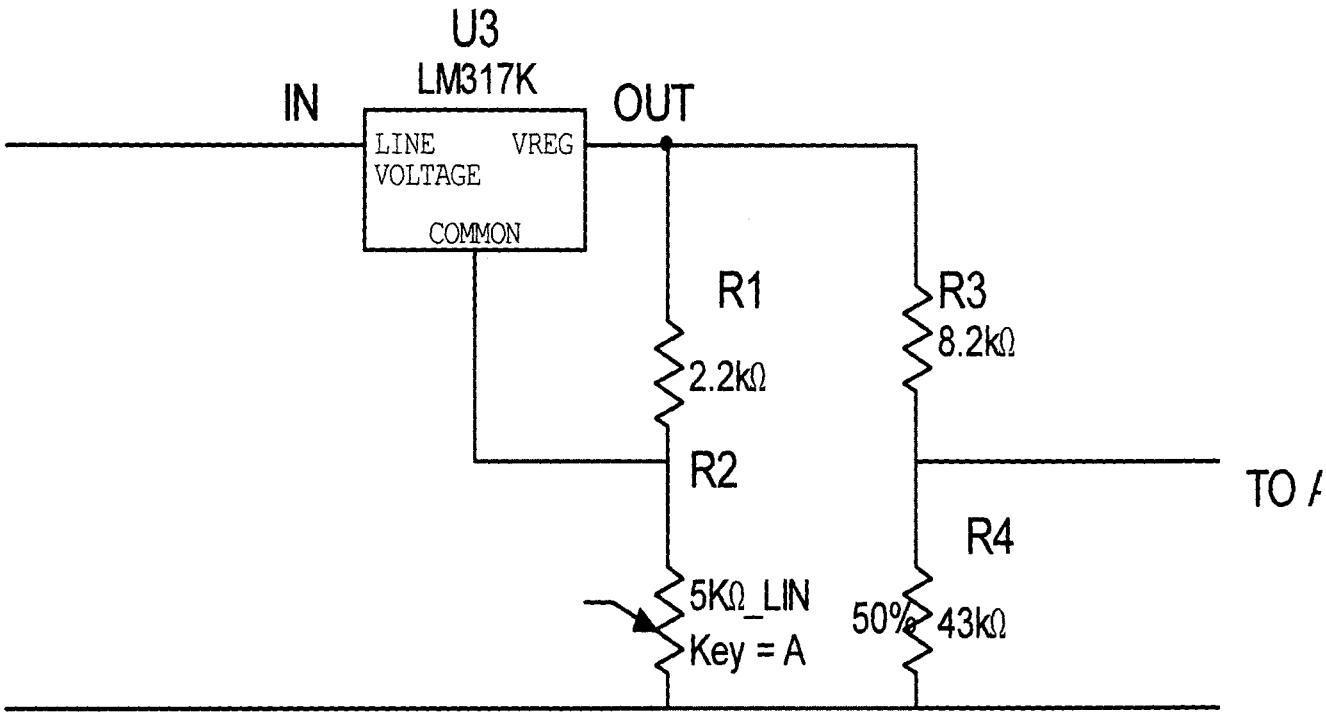

Fig 3.5 ADC input network R_3 , R_4 make up a 50kΩ preset resistance adjusted such that a ÷ 6 attenuation is obtained.

Using the potential divider formula ,

$$V_d = \frac{V_m \times R_4}{R_3 + R_4} \quad \text{.....(9)}$$

$$= \frac{V_{in} \times R_4}{50}$$

$$5 = \frac{30\,R}{50}$$

$$R_4 = \frac{250}{30} = 8.33K\Omega$$

$$R_3 = 50 - R_B = 50 - 8.33$$

$$= 41.66k\Omega$$

Software computation is effected to divide down the rectified voltage by 8.5 to derive the actual dc output voltage at 317T`s output.

3.4 8-BIT SYSTEM CONTROLLER

An AT89551 microcontroller is utilized as the system controller. The device was chosen for it s ample RAM space and versatile hardware functionality. The device has the following specifications listed below

Insert page 1 of AT89551 datasheet level .The device is interfaced with the ADC over P 1, a 3- digit 7- segment display over P 0 and the three digit controller over P2 . The system interface is shown below.

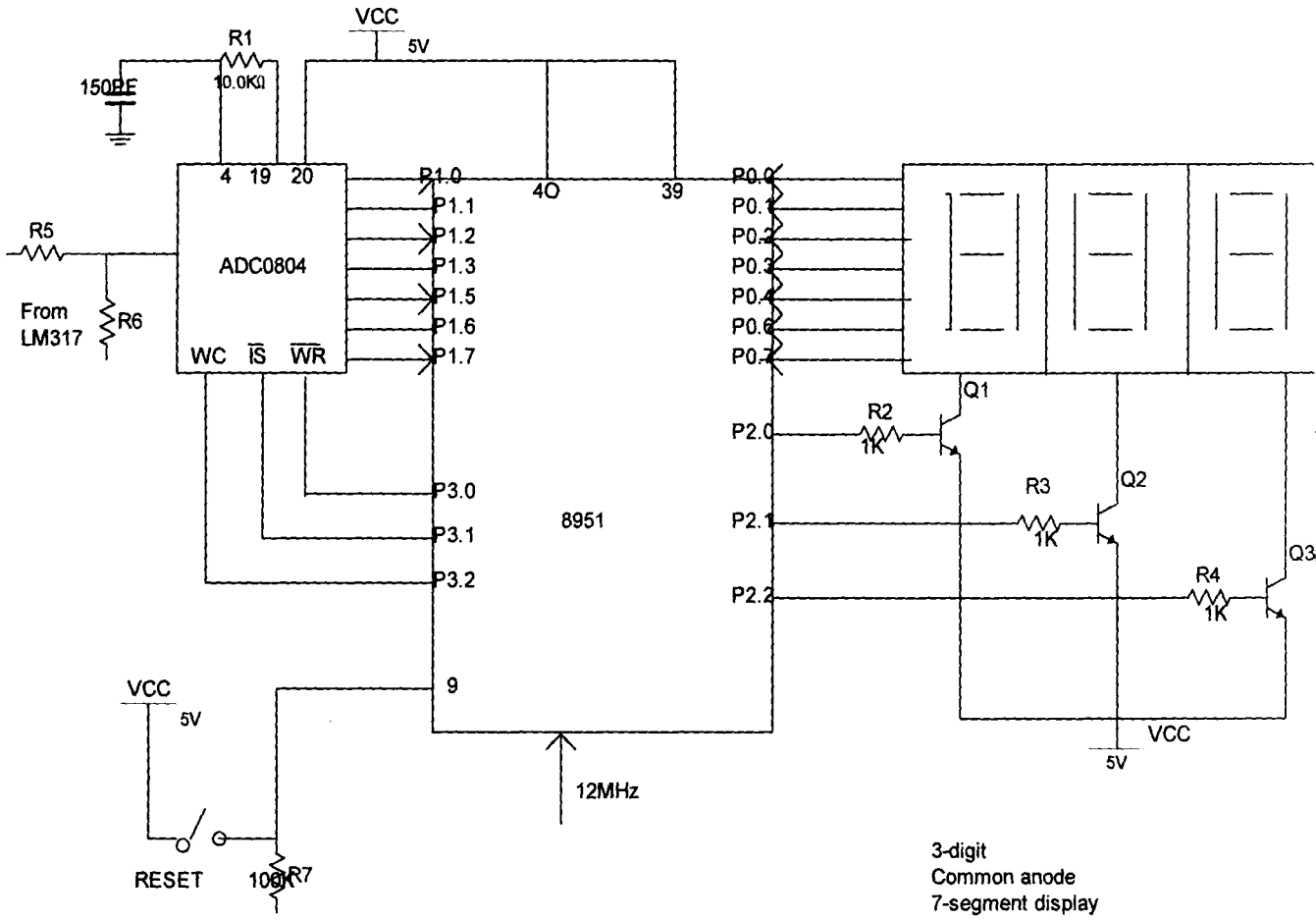

Fig 3.6 Microcontroller system interface

The controller is operated on a 12 MHZ crystal frequency yielding an instruction cycle time of 1μ sec . As the overall execution speed , this is deemed array enough .The 89X51 controls the 3-digit common anode 7-segment display over P 0 .A multiplexed analogue is used in which the segments is common to the three digits are tied together, i. e all `a` segments are tied together , all `b s` e. t. c . Individual display position control is effected via three PNP transistors interfaced to P 2 .

3.5 SEVEN SEGMENT DISPLAY

A common anode is used , the current that returns to ground is P 0

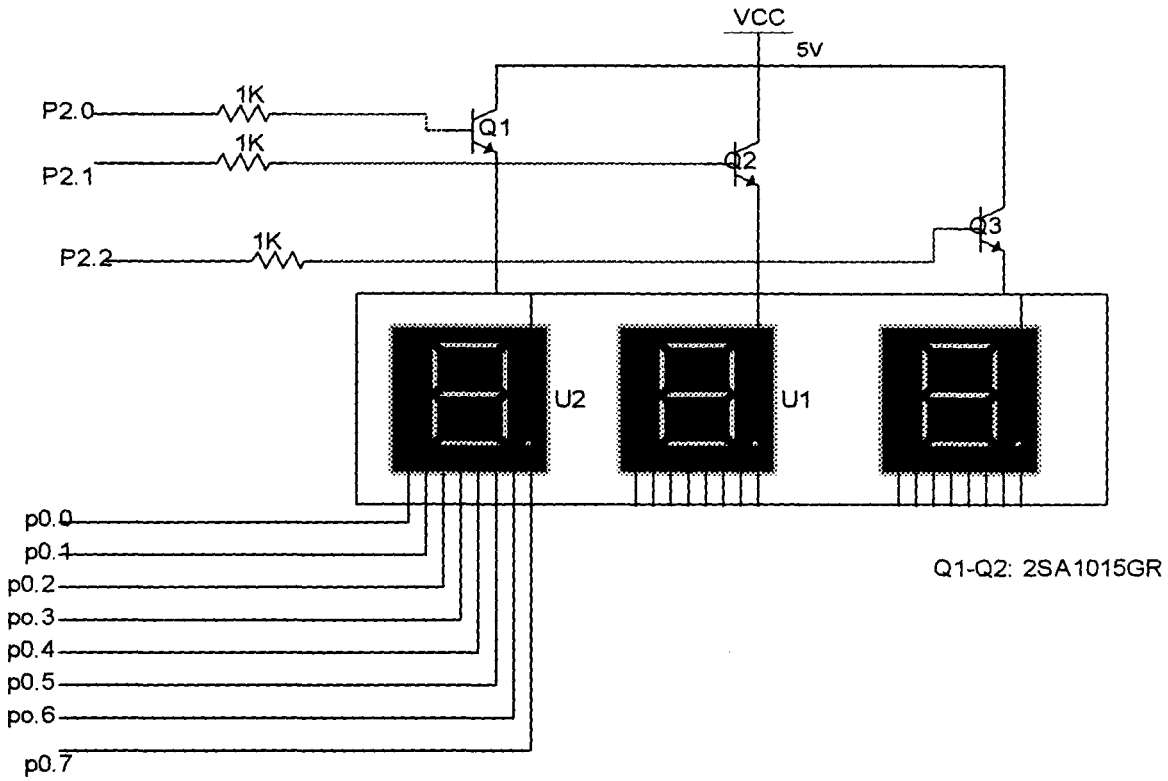

Fig 3.7 7 – segment display

Digit control is affected by turning on the PNP transistor associated with the desired digit position. For an n-digit multiplexed display, the total event flowing through each LED segment is I f, where I f is continuous LED forward current (5 ~ 20mA)

N = number of digits.

For a 3- digit display run at a continuous forward current of 20mili Amp , the total segment is;

3 x 20 = 60mA.

This value of current (60mA) is the current flowing through each segment .The peak digitcurrent

8x 60 = 480mA .

This value corresponds to the maximum peak current of each digit

The 2SA1015GR devices have an Ic of 150mA . Since the digit current is pulsed , the device Can handle a much higher Ic .

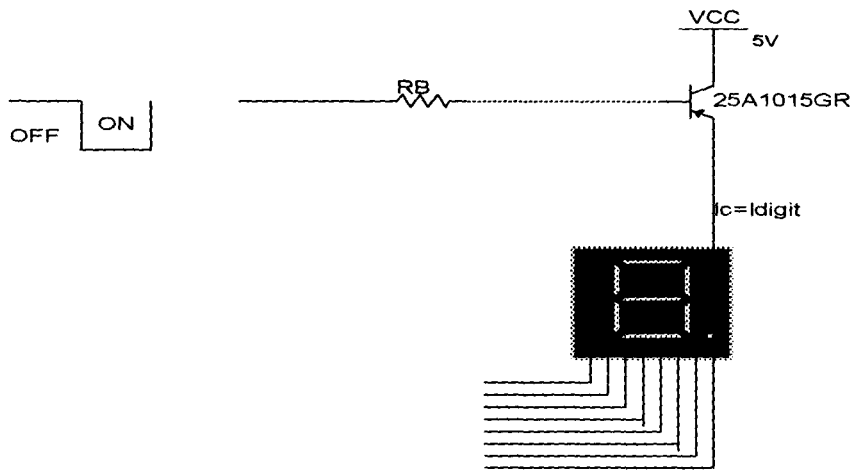

Fig 3.8 dc current gain

The 1015GR devices have a nominal dc current gain of 200

$I_C = 480$ m

$$I_B = \frac{I c}{H_{Fe}} \quad \ldots\ldots (10)$$

$$= \frac{480}{200}$$

= 2.4 milli Amp

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} \quad \ldots\ldots (11)$$

This module corrects the binary value of the voltage computation entries into BCD and subsequently to 7- segment code.Display refresh is effected using a software loop that continuously outputs the 7 – segment code of the data to displayed to P0 and turning on the digit diver associated with the digit position where the 7 – segment code is to be displayed .

The display is multiplexed, hence, a time –slot allocation of the common data path (P0) is effected. This is done by switching the digit divers

on /off in synch with the desired digit position.

The multiplexing arrangement involves;

1. Turning the three digit divers off.
2. Writing the 7 –segment code of the data to be displayed to the common data (Port PO).
3. Turning on the digit driver associated with the desired digit position.
4. Delaying a bit for data to be visible.
5. Turning off the previously on digit driver.
6. Repairing steps 1-5 for all desired digit position.

For a multiplexed 7-segment display, the amount of current through each segment is given by the expression:

$$I_{LED} = n * I_F \quad \text{.....(13)}$$

n = number of digits in the display

I_F = continuous LED forward current

I_{LED} = peak value of the current through each LED

A 3-digit display is used with the continuous forward current chosen to the

15mA.

$I_{LED} = 3 \times 15mA = 45mA$

Thus, 45mA flows through each LED in the display.

For a 7-segment ± display the peak current through each digit is then

8 x 45mA=360mA.

The digits are controlled by individual digit drivers as shown below.

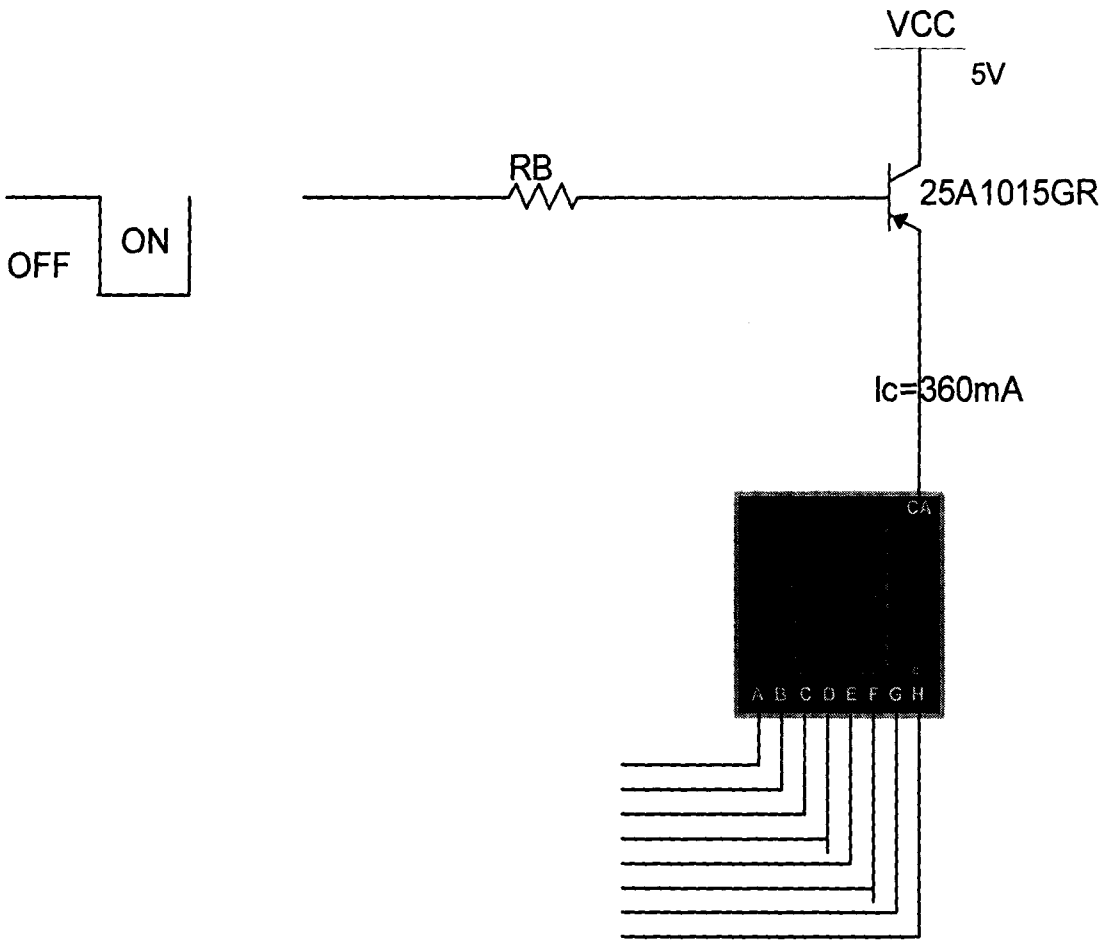

Fig 3.9, the transistor used as shown has a gain of typically 200.Rb is chosen to pass this value of collector current (360mA).

$$I_B = \frac{I_C}{H_{fe}} = \frac{3.6\times10^{-1}}{2\times10^{2}} = 1.8\times10^{-3}\ A \quad \text{.....(14)}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} : \frac{5-0.7}{0.0018} \equiv 2.4K\Omega \quad \text{.....(15)}$$

This value is halved to produce an acceptable brightness in the segments.

3.9 SOFTWARE REVIEW

The control software is coded in assembly language and is written to execute the entries that define the system functionality.

The control software consists essentially of the following blocks.

I. _System Initialization Block:

This block initializes the various system variables and sets-up the system hardware functionality.

II. The Analog-to-digital Conversion Block:

This block oversees the conversion of the voltage of the input of the ADC to a digital value

III._ Computation Block ;

Here, the digitalized value is processed to recover the desired information.

IV._Visual Display Block:

This block converts the binary data to the 7-segment equivalent to display.

CHAPTER FOUR

4.0 TEST AND RESULTS

The construction of a dc power pack with a digital readout has been carried out as follow;

After the purchasing of al the components being used in the design, a test was carried out in order to ensure that all the components are in good condition for use. For this matter, a digital meter as used.

The second stage of this design is that, the components layout for the system has been designed. Components were mounted on the bread -board which makes it possible to make some changes as the need arises and it makes it easier to locate bugs.

Having been satisfied with the behavior of the circuit, it was then transferred to the Vero - board; carefully, the components were soldered by means of soldiering iron and lead.

A 16-pin, 14-pin, 8-pin dual in line 1c, sockets was used to plug 1cs into the circuit. This way of connecting the Ic is of vital importance because it helps in troubleshooting enormously as the 1c is removed when making checks.

After the soldering has been completed, the entire circuit was carefully housed in a case (compartment). The case used discharges heat when working. To avoid system generating abnormal temperature, the power pack is kept in a ventilated area, for effective performance.

4.1 TESTING

When all the soldering is over, the circuit was traced and retraced to ensure that there is no short or open circuit anywhere. An original meter was used to test the continuity of the circuit. Making sure that the circuit has been soldered correctly, power was passed through it for testing purpose, the LED lights-up indicating that the power supply is ready for use.

LOAD (V)	OUTPUT DISPLAY (V)
2.70	2.70
3.50	3.50
2.95	2.95
4.50	4.50
4.60	4.60.

Table 3.0 output display of load applied

The construction of a dc power pack with a digital readout has been carried out as follow;
After the purchasing of al the components being used in the design, a test was carried out in order to ensure that all the components are in good condition for use. For this matter, a digital meter as used.

The second stage of this design is that, the components layout for the system has been designed. Components were mounted on the bread -board which makes it possible to make some changes as the need arises and it makes it easier to locate bugs.

Having been satisfied with the behavior of the circuit, it was then transferred to the Vero - board; carefully, the components were soldered by means of soldiering iron and lead. A 16-pin, 14-pin, 8-pin dual in line 1c, sockets was used to plug 1cs into the circuit. This way of connecting the 1c is of vital importance because it helps in troubleshooting enormously as the 1c is removed when making checks.

After the soldering has been completed, the entire circuit was carefully housed in a case (compartment). The case used discharges heat when working. To avoid system generating abnormal temperature, the power pack was kept in a ventilated area, for effective performance.

CHAPTER FIVE

5.0 CONCLUSION AND RECOMMENDATIONS

5.1 CONCLUSION

The power pack with a digital readout has been designed and constructed successfully not without hitches anyway. Some difficulties were encountered before the completion of this project. Among which is financial constraints, although, components used were readily available. The soldering on the circuit board was of great problem because so many ICS are involved.

5.2 RECOMMENDATIONS

Improvements can further be carried out on the DC power pack with a digital readout. One of the ways are basically as follows:

(i) Incorporating new ideas like powering the project using solar to actually actualize the project.

(ii) The output load range can be increased and hence, power handling capability by using specially moulded transformer that can give larger output.

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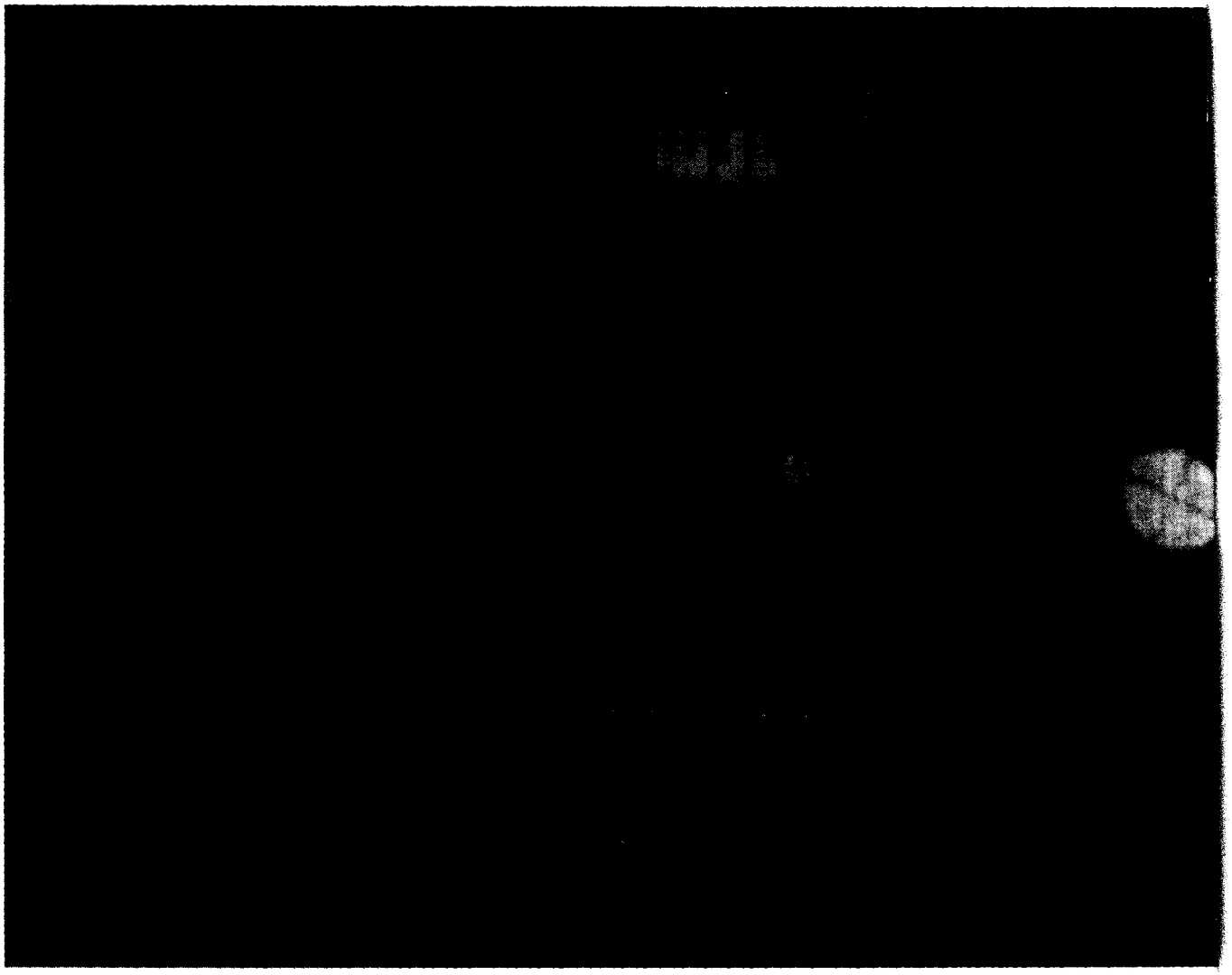
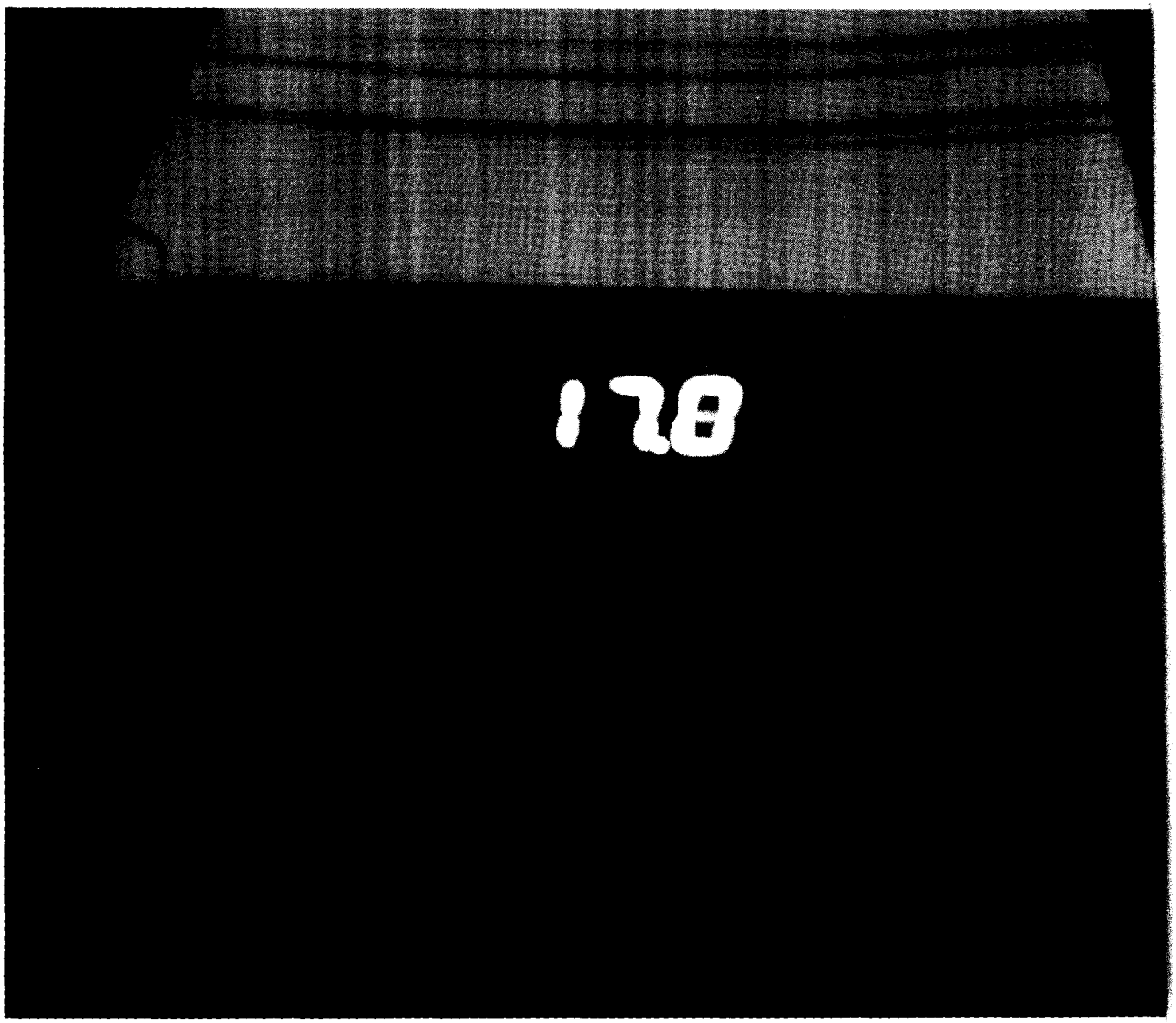
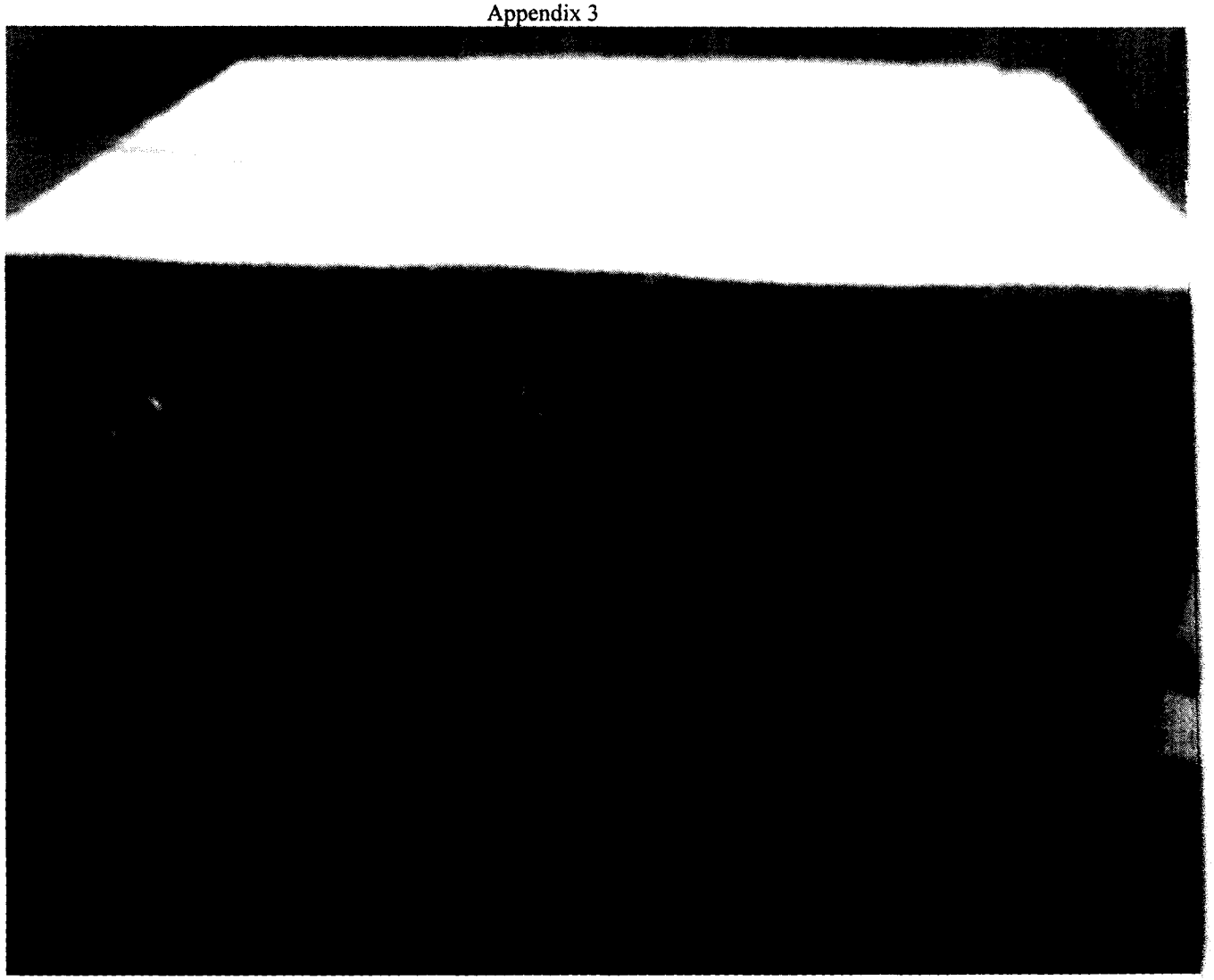
Appendix 1



Appendix 2



Appendix 3



Appendix 4

SOURCE CODE

```
INCLUDE 89C51.MC

DATA_PORT EQU P0
ADC_PORT EQU P1
ADC_SELECT BIT P3.0
ADC_WRITE BIT P3.1
ADC_INTR BIT P3.2
FREQ_OUT BIT P3.3
DIGIT_1_DX BIT P3.7
DIGIT_2_DX BIT P3.6
DIGIT_3_DX BIT P3.5
STACK EQU 40H
DIGIT_1 DATA 08H
DIGIT_2 DATA 09H
DIGIT_3 DATA 0AH
VOLTAGE_VALUE DATA 0BH
temp_a DATA 0ch
DX_PORT EQU P3


ORG 0000H
AJMP START_UP


ORG 000BH
        DJNZ R3, exit_isr
        MOV R3,#40
        CPL FREQ_OUT
exit_isr:       RETI


ORG 0030H
```

```
START_UP:   CLR EA
            MOV SP,#STACK
            ACALL SYS_INIT

MAINLOOP:   ACALL CONVERT_VOLTAGE
            ACALL PROCESS_VOLTAGE
            ACALL SHOW_VOLTAGE
            SJMP MAINLOOP

SYS_INIT:   ACALL RESET_DELAY
            ACALL reset_Delay
            ACALL reset_Delay
            ACALL reset_Delay

            MOV ADC_PORT, #0FFH
            MOV DX_PORT,#0FFH
            MOV TCON,#0
            MOV TMOD,#00000010B
            MOV TH0,#06
            MOV TL0,#06
            MOV R3,#40
            CLR ADC_sELECT
            MOV DPTR,#XLATE_tABLE
            MOV VOLTAGE_VALUE,#0
            ACALL PROCESS_vOLTAGE
            ACALL SHOW_VOLTAGE
            SETB TR0
            MOV ie,#10000010b
            SETB EA
            RET


RESET_dELAY:    MOV R7,#0
reset_loop:     MOV R6,#0
                DJNZ R6,$
                DJNZ R7, reset_loop
                RET

DELAY_2_SHOW:   MOV R2,#0
                DJNZ R2,$
                MOV R2,#0
                DJNZ R2,$
                RET
```

```
xlate_Table: DB
11000000b,11111001b,10100100b,10110000b,10011001b,10010010b,10000010b,11111000
b,10000000b,10010000b



CONVERT_VOLTAGE:    CPL p2.0
                    CLR ADC_wRITE
                    NOP
                    NOP
                    SETB ADC_wRITE
                    ACALL show_long
                    MOV VOLTAGE_VALUE,ADC_PORT
                    MOV temp_a, voltage_value
                    CLR adc_write
                    NOP
                    NOP
                    SETB adc_Write
                    ACALL show_long
                    MOV A, adc_port
                    CLR C
                    ADD A, temp_a
                    RRC A
                    MOV voltage_Value,A
                    RET

PROCESS_VOLTAGE:    MOV A, VOLTAGE_VALUE
                    MOV B,#5
                    DIV AB
                    PUSH B
                    MOV B,#10
                    DIV AB
                    MOV DIGIT_1,A
                    MOV DIGIT_2,B
                    POP ACC
                    MOV B,#10
                    MUL AB
                    MOV B,#5
                    DIV AB
                    MOV DIGIT_3, A
                    MOV A, DIGIT_1
                    MOVC A,@A+DPTR
                    MOV DIGIT_1,A
                    MOV A, DIGIT_2
```

```
                MOVC A,@A+DPTR
                MOV DIGIT_2, A
                MOV A, DIGIT_3
                MOVC A,@A+DPTR
                MOV DIGIT_3,A
                ANL DIGIT_2, #01111111B
                RET

SHOW_VOLTAGE:   MOV DATA_PORT,DIGIT_1
                CLR DIGIT_1_DX
                ACALL DELAY_2_sHOW
                SETB DIGIT_1_dX
                MOV DATA_PORT,DIGIT_2
                CLR DIGIT_2_DX
                ACALL DELAY_2_sHOW
                SETB DIGIT_2_DX
                MOV DATA_PORT,DIGIT_3
                CLR DIGIT_3_DX
                ACALL DELAY_2_SHOW
                SETB DIGIT_3_dX
                RET


show_long:      MOV R1,#25
show_loop:      ACALL show_voltage
                DJNZ R1, show_loop
                RET
```

Appendix 5 Complete Circuit Diagram