DESIGN AND CONSTRUCTION OF DIGITAL ELECTRONIC BALLOT MACHINE

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CERTIFICATION

This is to certify that this work title ***Design and Construction of Digital Electronic Ballot Machine*** was carried out by **Samaila Elijah Danjuma**, under the supervision of Engr. Emmanuel Eronu for the award of Bachelor of Engineering in Electrical and Computer Engineering department, Federal University of technology, Minna.

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External Examiner

Date/Signature

DECLARATION

I, ***samaila Elijah Danjuma*** hereby declare that the idea and execution of this project was carried out by me, under the supervision of ***Engr. Emmanuel Eronu*** of Department of Electrical and Computer Engineering, Federal University of Technology, Minna.

Signature of Student

30TH OCTOBER, 2003
Date

DEDICATION

I dedicate this project to the Almighty God, for His guidance and protection over my life throughout my course of study as well as making this project a reality.

ACKNOWLEDGEMENT

My special thanks and reverence goes to the almighty God who in His infinite mercy saw me through every endeavour and challenge I undergone in the system.

My profound gratitude goes to my beloved mother in person of Mrs. Deborah, brother Joshua, brother Isaiah, sister Felicia, Mrs. Solomon, Pastor Solomon John and other relatives for their advice and financial assistance.

I greatly acknowledge the technical guidance and moral support from my project supervisor, Engr. Emmanuel Eronu and my head of department, Engr (Dr) Y.A Adediran at various times.

I acknowledge with gratitude the contribution of my brother Babalola Ebenezer, brother Fafemi Adebola, brother Dayo and brother Seun for their endless contribution to the successful completion of my project.

My gratitude also goes to brother Andrew A. Adutu and brother Simon Samuel for their contribution in cash and kind towards completion of this project work.

I can not afford not to acknowledge the unforgetable effort of brother Dayo Ofusori towards the success of this write up by CMOS data sheet materials provision and brother Jonathan Ibrahim for making His system unit available for me to be used throughout the typing of the project.

May the Almighty God reward you all (amen).

ABSTRACT

Little or no technological advancement couple with the geometric increase in population associates with usual ballot process has made the hostel accommodation ballot exercise practised by underdeveloped countries universities inefficient, slow and unattractive. Nigeria falls into league of such countries.

To move away from this archaic system, technology must be adopted to automate the hostel accommodation ballot exercise in Nigeria universities.

It is on this note that I thought it wise to design and constructs a ***Digital Electronic Ballot Machine*** as an introduction to the automation of the hostel accommodation ballot process in Nigeria universities which if developed and delivered to the appropriate universities ballot officials will help curtail inefficiency in the hostel accommodation ballot exercise and ease the task of archaic labour as well as increase the efficiency and speed during the exercises.

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CHAPTER ONE

GENERAL INTRODUCTION

1.1 INTRODUCTION

Owing to the consistence increase in the population of students in institution of higher leanings with inadequate hostel accommodations in underdeveloped countries Nigeria, hostel accommodation ballot exercise has become one of the adopted practice in the system.

Ballot has to do with the process of selecting or picking a choice out of numerous or different options. The option could be applied to human being as in the democratic open ballot system, or probability of occurrence like head or tail or *Yes* or *No* as in the hostel accommodation ballot system of institution of higher leaning.

However, my design is only concerned with the ballot of probability of occurrence; that is, a process whereby papers are cut into smallest sizes and *Yes* or *No* is written on them for students to pick. If a student pick the paper written *Yes*, then He or She is qualified to secure accommodation in the hostel while the student who unfortunately pick the paper written No will not be entitled to secure hostel accommodation for that session. With the above stated, many students end up in not having chance to ballot while on the queue till the exercise stops because of the time spend in paper picking as well as counting the number of yes being picked and the compatible act of the ballot officials.

Therefore, the automation of ballot process in Nigeria higher institution of learning has become necessary or else, it will be difficult to meet up the challenges of the new era as seen in the ever increasing population of the nation universities.

The design and construction of the digital electronic ballot machine is an introduction to the automation of ballot process that will help in reducing the fraudulent acts, easing and reducing the task of counting and evaluation.

1.2 PROJECT OBJECTIVE/MOTIVATION

The design and construction of the digital electronic ballot machine is aimed at:

- Reducing fraudulent acts and other vices that could arise during ballot exercise.
- Easing and reducing the task of ballot officials during practise and evaluation of figures.
- Introduction of automation in ballot process to meet up the challenges of the new millennium as seen in the ever-increasing population of any higher institution of learning of under developed nations.
- Saving time during ballot exercise.

1.3 LITERATURE SURVEY/REVIEW

At the beginning of the university system in Nigeria, many years ago, the issue of ballot for hostel accommodation was not in practice, because there was enough hostels for students, as a result of the few number of students in the school.

As time goes on, the rate of admission into the universities started exceeding that of the grandaunts and the university authorities could not provide adequate accommodation for the large population they offer admission into the universities, for every body wants to go to school.

At this point, the issue of ballot has to be introduced to the system to accommodate the few that are fortunate to pick Yes during the ballot exercise as earlier stated in the introductory part of this chapter, among the large population of students in the school.

In this case, technology has to be harnessed to automate the ballot process to help meet up with the challenges of the new millennium. It is on this basis that I opted to harness the use of electronic device known as ***Digital Electronic Ballot Machine*** as an introduction to the automation of hostel accommodation ballot process.

This will, to some extent, prevent ballot vices like fraudulent act of the ballot officials and so on during the exercise. This system works on the principle of latch, execute, and reset mode.

As a student press the set button, the oscillator triggers the counter and operate the control section or panel, which results into a cycle oscillation of 16 binary codes. The memory latch and allow the switch to access just one binary code from the counter to the memory during the rapid cycle, and the code is linked to the 4 input and 16 output bits decoder, the 4-bits binary code allows one of the decoders output to be logic 1 of high in order for a signal to be sent to the display unit to display the option that is linked to the code via the OR gates and the selector AND gates.

But, we are only interested in YES display; therefore all the Yes codes are sum up using OR gates, so that whenever, Yes code is access, the output of the OR gate is high or logic 1. This leading logic 1 would then triggers the Yes counter, so that Yes can be recognized with a count as well as the display, while only the display is use to identify No.

1.4 PROJECT OUTLINE

This project write-up is a report on the design, construction and testing of the ***Digital Electronic Ballot Machine***.

The first chapter gives a general introduction of the project, the project objectives/motivation and the literature survey or review. The second chapter deals with the systems theory, design and calculation of components used in the project work.

The third chapter gives an insight on the integrated circuit and choice of logic family used, construction techniques and step by step testing of each of the modules that make up the overall circuit as well as other construction materials involved in the project construction and the system device operation.

While the last chapter deals with the discussion, conclusion and recommendation for future improvement of the work done with a reference to all theoretical work.

CHAPTER TWO

SYSTEM'S THEORY, DESIGN AND CALCULATION

2.1 PRINCIPLE OF OPERATION

Fig 2.1 shows the block diagram of the ***Digital Electronic Ballot Machine***

The system consist of 8 basic units as shown below

- The power supply unit
- The oscillator unit
- The counter unit
- The latch 14 – 16 decoder unit
- The yes – no logic selector circuit unit
- The controller unit
- The yes counter unit
- The Yes/No display unit

The power supply unit activates and supplies power to other units.

The oscillator unit is meant for triggering the four input – 16 codes counter as well as activating or clocking the mini controller section and aid the effective display of yes or no in the display unit of the entire circuit.

The oscillator unit consists of a 4060B square wave generator connected to an RC oscillator. As the power supply unit activates the oscillator unit, a square wave is generated. The generated wave is then divided into ten waveforms of different frequencies level with the aid of the divider in the 14 –

Stage Ripple Carry Binary Counters (4060B), while the RC oscillator is working at about kHz.

The frequency of the different waveforms generated includes: 512Hz, 256Hz, 128Hz, 64Hz, 32Hz, 16Hz, 8Hz, 4Hz, 2Hz and 1Hz and 1Hz.

As the power supply unit activates the oscillator unit, the RC oscillator triggers the 4520 dual synchronous up counter and makes it to count from 0000 to 1111 at a frequency of 128Hz.

During the rapid cycle of the counter, the latch in the 4514 decoder access just one binary code at a time from the counter, register it in its memory and kink it to the input lines of the decoder.

As the bits of the code gets to the decoder, it allows one of its outputs corresponding to the input code to be logic 2 or high.

The yes codes are sum up using eight input, four (4) input and two (2) input OR gates to represent 8 yes, 4yes and 2 yes respectively. The output of each OR gate was linked to a two input AND gate, while the remaining codes that are not linked to either of the gates represent the "0" yes in order to make the project a selector programmable.

The three (3) two (2) input AND gates are sum up using a three input OR gate so that one of the three AND gates is enabled at a time while others are disabled via the selector. Whenrever a yes code is accessed, the output of the OR gate is high or logic 1.

This leading logic is then used to activate the yes counter unit and the yes display unit, so that yes can be recognized by a count and the YES display.

The mini controller sub section controls the operations of the 4514 decoder, the delay as well as the display register D flip flop by selecting each of the sub units at a time as it cycle through itself so that the yes counter and the display units are activated at an interval of 2 seconds each time the ballot button is pressed.

The display unit displays yes or no according to the code accessed from the counter unit, while the yes display counter count the number of yes picked.

The system is designed to accommodate as much count as 999.

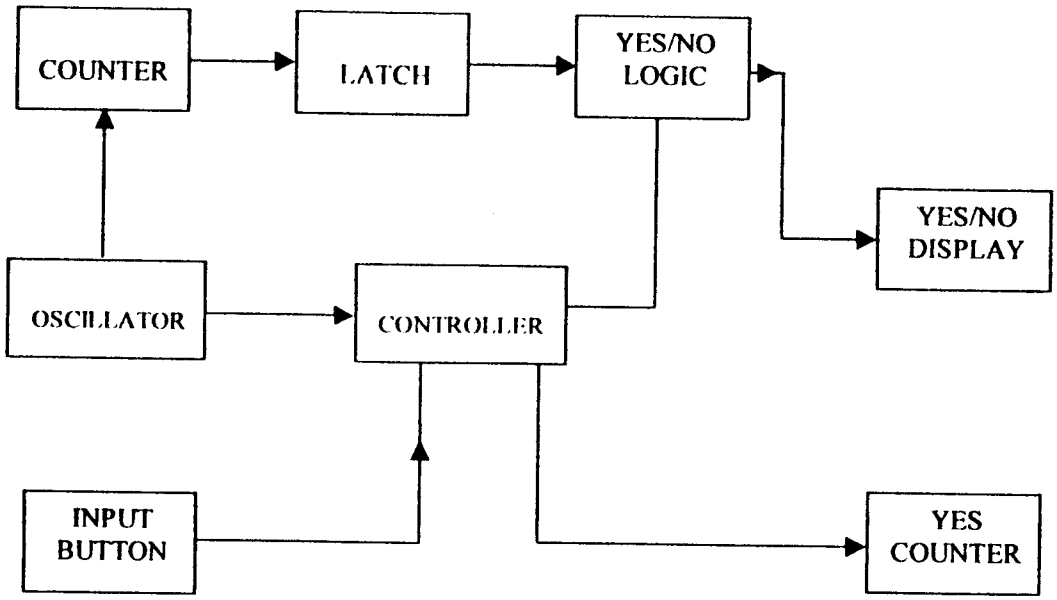


Fig 2.1: ***Block Diagram***

2.2 POWER SUPPLY UNIT

Direct current is usually needed in almost all electronic circuits or system for their operation. Dry cell are one form of DC source but their voltage cannot be maintained for a long time. Therefore, the most convenient and

economical source of power is the domestic alternating current supply where alternating voltage (usually 240V r.m.s) is converted to desired DC voltage. This process of converting AC voltage to DC voltage regulating circuit to help maintain a constant voltage across the load. The diagram below put together constitutes the regulated power supply unit.

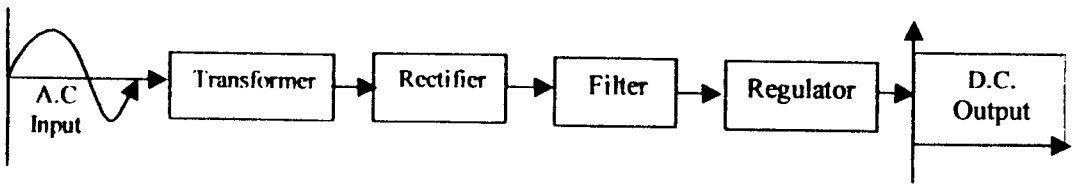


Fig. 2.21: BLOCK DIAGRAM OF A REGULATED POWER SUPPLY UNIT.

2.21 THE TRANSFORMER

The transformer is a device that steps the domestic AC supply of about 240 Vrms to the required voltage that suits electronic devices.

The transformer consist of two closely coupled coils called primary and secondary; an AC voltage applied to the primary (Vp) appears across the secondary (Vs) with a voltage multiplication inversely proportional to the turn ratio. The voltage transformation ratio (K) tells whether it is step–up or step-down.

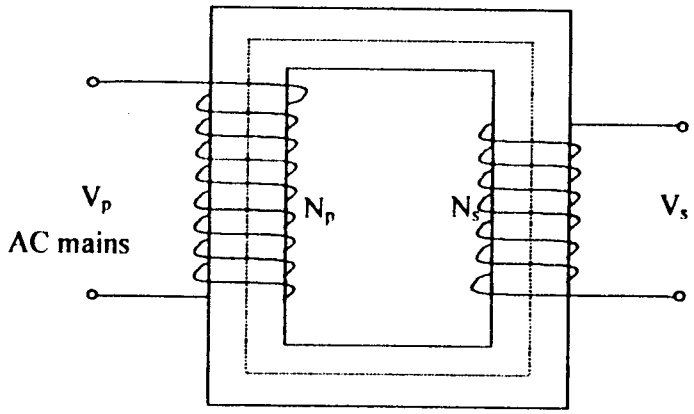


Fig 2.22: ***THE TRANSFORMER***

$K = Vs/Vp = Ns/Np$

For an ideal transformer

$1/k = Vp/Vs = Is/Ip$

When $k > 1$, the transformer is a step–up

When $k < 1$, the transformer is a step–down.

K = voltage transformation ratio

Vp = voltage applied at the primary coil

Vs = Voltage delivered at the secondary coil

Np = Number of turns in the primary coil

Ns = Number of turns in the secondary coil.

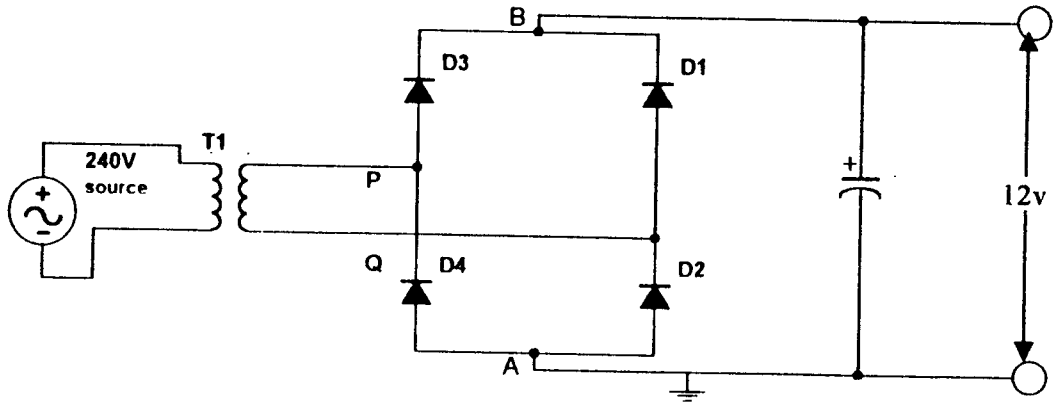
However, a 12V step –down transformer was choose for this project because, the device required a nine volt (9V) supply to be powered.

2.22 THE RECTIFYING CIRCUIT

Rectification is a process where by an alternating voltage is converted to a pulsating direct voltage by employing one or more diodes. The circuit connection that does this is known as the rectifying circuit.

For this project, a full-wave bridge rectifying was used due to the fact that it has less ripple, and produces twice as much output voltage of the three (Half–wave, full–wave and full–wave bridge) rectifications.

Also, the average current through a diode in full wave rectification equals only half the D.C load current because there are two diodes in the circuit, each sharing the load.



D1=D2=D3=D4=1N4002

Fig. 2.23: A FULL WAVE BRIDGE RECTIFYING CIRCUIT

During the positive input half–cycle, terminal p of the secondary is positive while Q is negative.

Diodes D1 and D3 are forward–biased (ON) while D2 and D4 are reverse–biased (OFF); hence, current flows round the load.

During the negative input half–cycle, secondary terminal Q is positive while P is negative. However, D2 and D4 are forward–biased while D1 andD3 are reverse biased, so current also flows round the whole circuit. Hence, current keeps flowing during both half–cycles of the AC input supply.

The average DC voltage of the output voltage is given by he equation below:

$$V_{dc} = 2\frac{2V_r}{\pi} = \frac{2\sqrt{2}}{\pi} V_s$$

Where V_P and V_S are the peak and r.m.s value of the rectifier input voltage.

2.23 THE FILTERING CIRCUIT

Owing to the fact that, the output voltage of the rectifier consist of ripples, a filtering circuit is required to remove the ripple contents.

The filtering is achieved by passing the rectified voltage through a capacitor. For this device, a 2200μF was used.

The capacitor charges up during the diode conduction period to the peak value and discharges through the load when the rectifier voltage falls below the peak value.

The filter capacitor is chosen large enough to provide acceptably low ripple voltage. The capacitor is polarized in order to provide high values of capacitance in small packages. The figure below shows the diagram of the filter action.

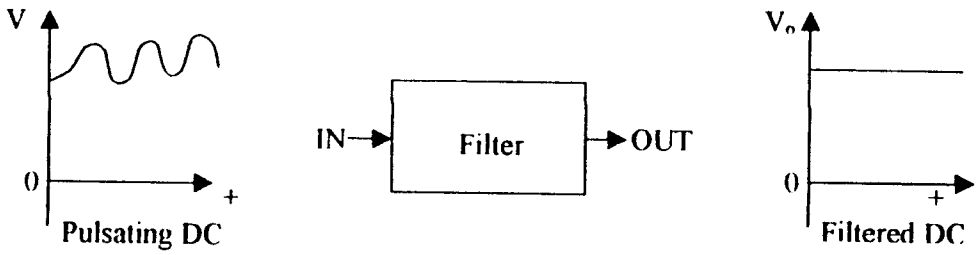


Fig. 2.24(a): DIAGRAM OF THE FILTER ACTION

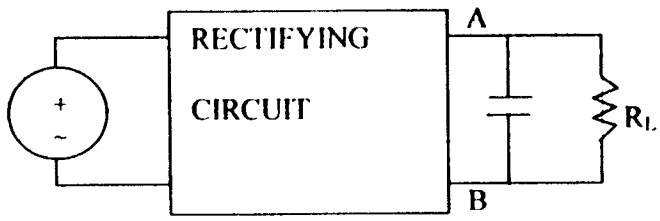


Fig 2.24(b) DIAGRAM OF THE RECTIFYING CIRCUIT

2.24 THE REGULATOR

To ensure the constant supply of voltage, that is, 9Vpowering the whole circuit to avoid damage of the components, a regulator is required for the task.

Thus, a positive 9V regulator was used, while a capacitor was connected across its output terminal to improve the transient response.

2.25 DESIGN SEQUENCE OF THE SUPPLY UNIT

Almost all of the ICs used in this project are powered by voltage below 9V supply and draw current in the range of micro and milli Ampere (μA and mA). Hence, a 9v power supply that can deliver 1A is designed for it.

A transformer voltage of 12v was used.

$V_{peak} = V_{peak} = V_{rms}\sqrt{2}$

$V_p = 12V$

$V_{rms} = V_p/\sqrt{2} = 12v/\sqrt{2} \simeq 9.0V$

For constant supply of V_{rms} value, the 12V transformer is suitable for the project. A fuse necessary to protect the circuit against current surges was installed at the primary side of the transformer.

For an ideal transformer

Power input = power output

$P = IV$

$I_pV_p = I_sV_s$

From above, $Vp_{(rms)} = 240V_p$, $V_{s(rms)} \simeq 9.0V$

$I_s = 1A$ (chosen)

$I_p = I_sV_s./V_p = 1X\ 9.0/240. \simeq 38A$

Thus, at full load, a current of 38mA flows in the primary coil of the transformer. However, by considering the heating effect of the primary current, current surge, filtering action of the capacitor and allowance for the fuse at full load,

Fuse rating = 38mA X 6(allowance for current surge) X 2(heating effect) X 2(allowance for fuse under excess load)

$= 38mA\ X\ 6\ X\ 2\ X\ 2$

$= 0.912 \simeq 1A$

therefore, a slow –blow fuse of current rating of 1A was connected at the primary side of the transformer.

To calculate the peak inverse voltage (PIV) of the diodes of the bridge rectifiers:

$V_{peak} = 12V$

V_{dc} = average D.C voltage

$V_{dc} = 2V_{peak}/\pi$ _ For a full wave rectifier,

$V_{dc} = 2X12V/\pi = 7.64V$

$V_{dc} \simeq 8V$

Thus, diodes of PIV rating greater than 12V with a forward current rating of 1A were chosen for the rectification.

Based on estimation, the ripple voltage of the rectifier output was about 9V.

For V = ripple voltage,

That is, V = 9V

Let Δt = time between peaks of the rectified input waveform.

Δt = 1/2f, f = frequency of the mains = 50Hz ..

=1/2x50=10mS

recalled, $I = C\Delta_v/\Delta_t$

let I = 1A (chosen)

$C = I\Delta_t/\Delta_v = 1x10mS/9...$

$C \simeq 1.1mF = 1100\mu F$

2.3 OSCILLATOR UNIT

Different oscillators are required for the triggering of the four input – 16 codes counter, the clocking of the mini controller section and the display of yes or no in the display unit; However, to save the cost of buying many oscillators, a CMOS 4060B Ripple Carry Binary Counter that could generate different oscillatory frequencies is required to undertake the task. Although, there are other Ripple Carry Binary Counters like 4020B 14 – stage Ripple Carry Binary Counters, 4040B 14 - Stage Ripple Carry Binary Counters, that could be used for this project, but 4060 was chosen because, it is readily available in the market.

2.31 THE 14 STAGE RIPPLE CARRY BINARY COUNTER

The 4060B is a 14 - stage ripple carry binary counter that is advanced one count on the negative transition of each clock pulse. The counter is reset to the zero state by a logical 1 at the reset input independent of clock. The counter is also a square wave generator containing a divider and an RC oscillator.

Whenever a square wave is generated, the divider divides the generated waveforms into 10 different oscillatory frequencies conforming to the RC oscillator frequency of about 1KHz.

Supply voltage range	1v – 15v
Noise Immunity	$0.45V_{DD}$ typ
TTL Compatibility	fanout of 2 drving 74L or ! driving 74LS
Speed of operation	8MHz typ. At V_{DD} = 10V

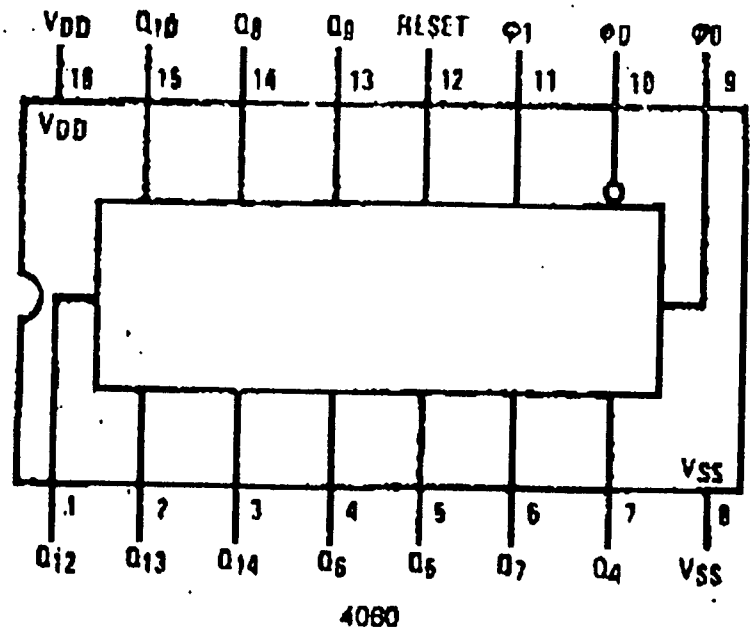


Fig 2.31 INTERNAL CIRCUIT OF THE 14 STAGE RIPPLE CARRY BINARY COUNTER

2.4 THE COUNTER UNIT

Counters are device, which record the number of pulses applied to their input. The basic component of a counter is the flip – flops that can be connected in various arrangements to function as binary counters that count input clock pulses.

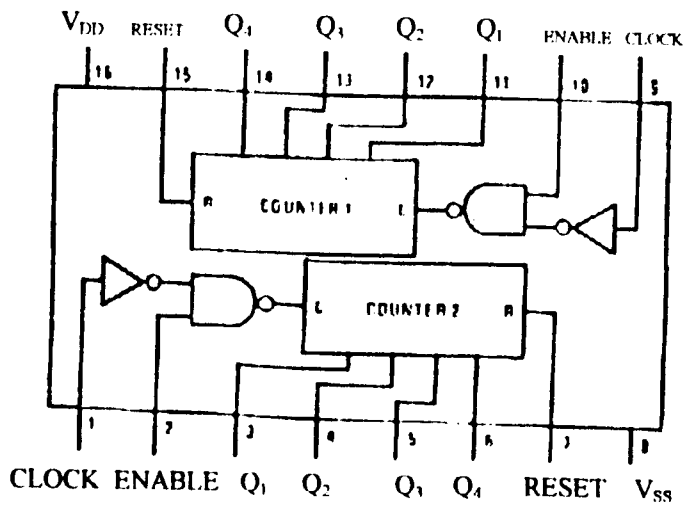
Digital counters can be designed to have the following features, modulus, up and down counters, synchronous or asynchronous operation, free running or self-stopping. The counter unit consist mainly the 4520B dual synchronous up counter. The counter was chosen because of its ability to count from 0000 to 1111 and makes accessing of any of the 16 codes easy via the 4 input – 16 – codes decoder.

2.41 THE DUAL SYNCHRONOUS UP COUNTER

The 4520B dual synchronous binary up counter is implemented with complementary MOS (CMOS) circuit constructed with N – channel and P – channel enhancement mode transistors. Each counter consists of two identical, independent, synchronous, 4 – stage counters. The counter stages are toggle flip – flops that increment on either positive – edge of clock or negative – edge of enable, simplifying cascading of multiple stages. A level on the reset line can asynchronously clear each counter. All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Supply voltage range	3v – 15v
Noise Immunity	$0.45V_{DD}$ typ
TTL Compatibility	fanout of 2 driving 74L

Counting rate (typ) at V_{DD} = 10V 6MHz



4520

Fig 2.41 THE CIRCUIT DIAGRAM OF THE DUAL SYNCHRONOUS UP COUNTER

2.5 THE LATCH/4 – 16 DECODER UNIT

The latch/4-16 decoder unit is made up of the 4 bit latch/ 4 – to – 16 line decoder that is responsible for the accessing of a code to be registered at the latch or memory during the rapid cycle of the dual synchronous up counter and the decoding of the code as well as linking it to the YES – NO LOGIC SELECTOR CIRCUIT unit. The decoder was using to save the cost of buying separate latch for this unit.

2.51 THE 4 BIT LATCH/ 4-to-16 LINE DECODER

The 4 bit latch/4-to-16 line decoder is a logic circuit that accepts a set of inputs that represents a binary number and activates only the output that corresponds to that input number. In other words, the decoder circuit looks at

its inputs, that is, the code it access from the counter and store or register it in its latch.

The decoder then determines the decimal number equivalent of the code and activates only the output(s) corresponding to the number (decimal).

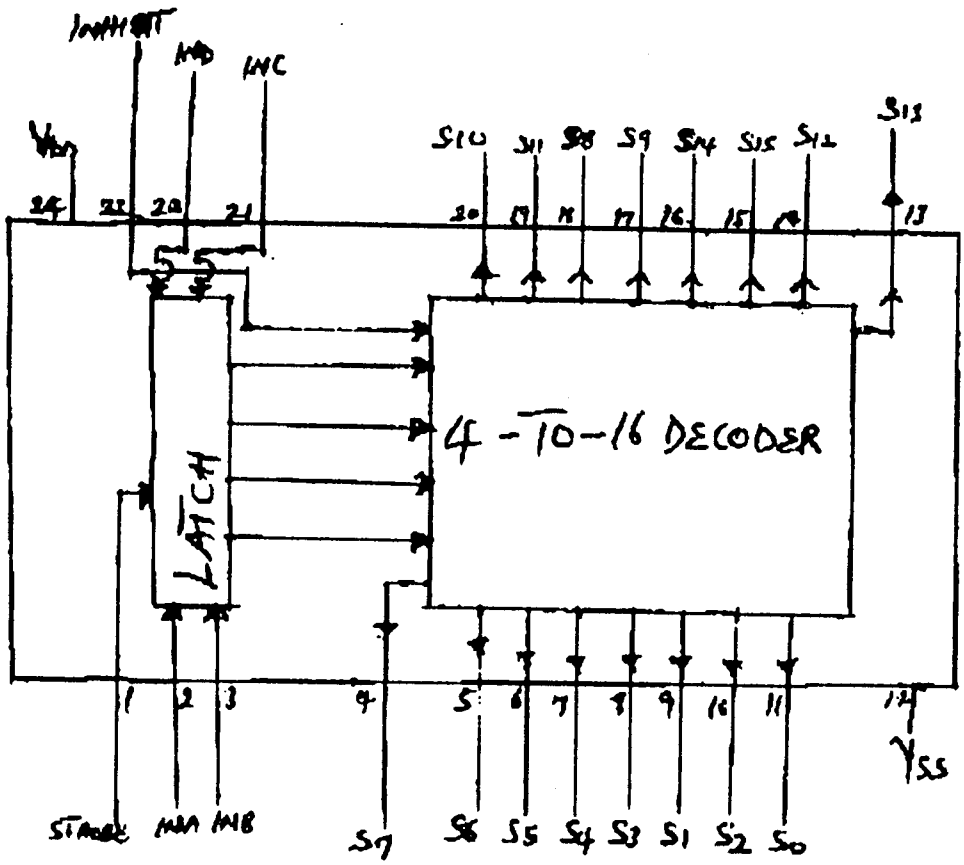


Fig 2.51 THE CIRCUIT DIAGRAM OF THE 4 BIT LATCH/ 4 – TO – 16 LINE DECODER

2.6 THE YES – NO LOGIC SELECTOR CIRCUIT UNIT

The YES – NO logic selector circuit unit comprises the eight (8) input, four (4) input, two (2) input, three (3) input OR gates, the selector, the Four Two (2) input AND gates and an inverter. The outputs of the latch decoder were linked to the 8, 4 and 2 input OR gates to serve as their inputs according to the probability of the YES codes that could be activated at its outputs during the ballot exercise.

Each output of the OR gates are also linked to three of the two (2) input AND gates, that is, one for each of the outputs of the eight input, four input and two input AND gates to be enabled by the selector at a time. This implies that whenever one of the AND gates is enable, the other two will be disabled, so that only the code linked to the activated gate will display YES via the YES display unit as the high output of the gate passes through the three input OR gate and activates the YES counter display unit as well as the sound unit.

The inverter, that is, 4069B, which consists of six inverter circuits, was used to implement all general-purpose inverter applications in both the selector subunit and the entire circuit.

2.61 THE OR GATES

In digital circuitry, OR gates are circuit that have two or more inputs and whose outputs are equal to the OR sum of the inputs.

In other words, the OR gates operates in such a way that their outputs are HIGH (logic 1) if either one or all of their inputs are at a logic 1 level.

In each of the OR gates used, the output will be LOW (logic 0) only if all of their inputs are at logic 0. Below is the truth table defining the OR gates operation and the circuit symbol for the OR gates used.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Fig 2.61A: THE TRUTH TABLE DEFINING AN OR GATE OPERATION

Fig 2.61B: circuit symbol for the two input "OR" gate

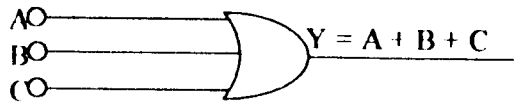


Fig 2.61C: circuit symbol for the three input "OR" gate

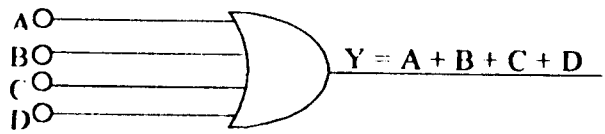


Fig 2.61D: circuit symbol for the four input "OR" gate

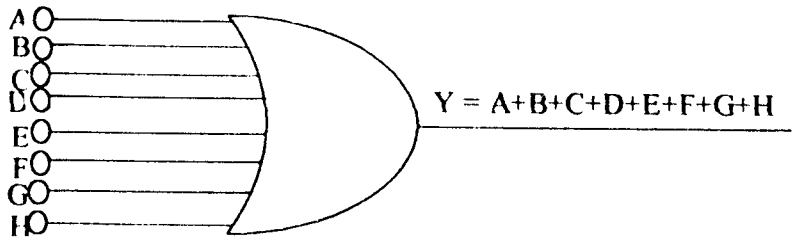


Fig 2.61E: circuit symbol for the eight input "OR" gate

2.62 THE AND GATES

The AND gates are circuit that have two or more inputs and whose outputs are equal to the AND product of the inputs; that is, Z = AB for two input AND gate. In other words, the and gates are circuit that operate in such a way that their outputs are high only when all of their inputs are HIGH, while the outputs are LOW for all other cases. The truth table defining the AND gates operation and the circuit symbol for the AND gates used are shown below.

A	B	Z A.B
0	0	0
0	1	0
1	0	0
1	1	1

Fig. 2.62A *THE TRUTH TABLE DEFINING "AND" GATE OPERATION*

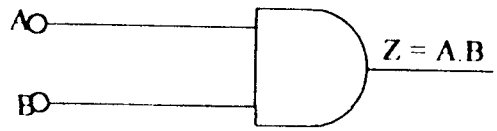


Fig. 2.62B *CIRCUIT SYMBOL FOR THE TWO INPUT AND GATES*

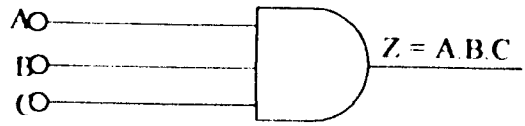


Fig. 2.62C *CIRCUIT SYMBOL FOR THE THREE INPUT AND GATES*

2.63 THE 4069 INVERTER CIRCUIT

The 4069 consists of six inverter circuits as said earlier and is manufactured using complementary MOS (CMOS) to achieve wide power-supply operating range, low power consumption, high noise immunity and symmetric – controlled rise and fall times.

The device is intended for all general -purpose inverter applications where special characteristics of the 74C901, 74C903, 74C907 and 4049 hex inverter/buffers are not required. In those applications requiring larger noise immunity, the 74C14 or 74C914 hex Schmitt trigger is suggested.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

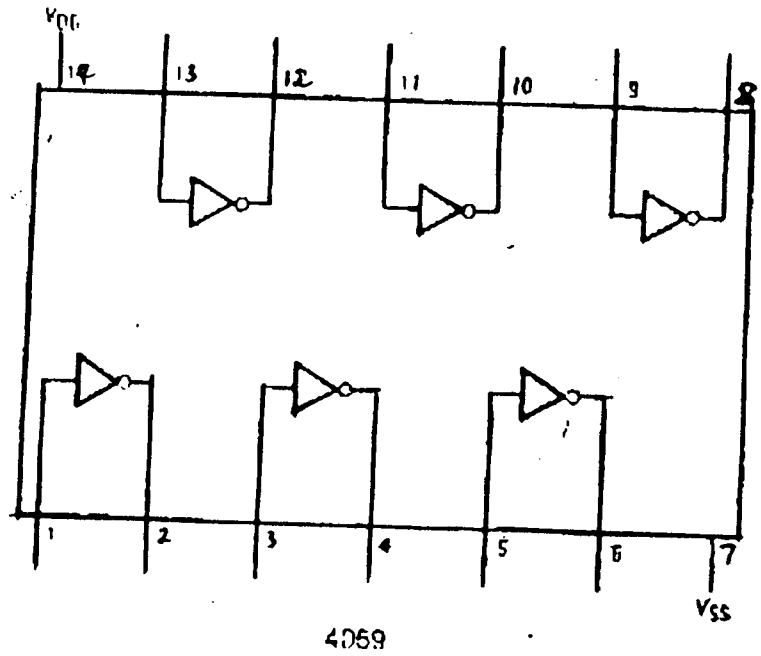


Fig 2.63: THE 4069 INVERTER CIRCUIT

2.64 THE SELECTOR

The selector is made up of a 4022B divide by 8 Counter/Divider with 8 Decoded outputs which switches the Resistor Transistor Logic driver/buffer connected to the Light Emiting Diodes (LEDs) that display three different kinds of light colour according to the probability of YES to be displayed out of the sixteen codes AND gate selected. For example, the green, red and yellow lights are displayed whenever the AND gates for the eight (8) YES, four (4) YES and two (2) YES respectively are enabled. The 4022B is a 4 – stage divide –by – 8 Johnson counter with eight decoded outputs and a carry – out – bit.

The counters are cleared to their zero count by a logical 1 on their reset line and advanced on the positive edge of the clock signal when the clock enable signal is in the logical 0 state.

The configuration of the 4022B permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical 0 state and go to the logical 1 state only at their respective time slot. Each decoded output remains high for one full clock cycle, that is, the 4022B is a stepper that advances logic 1 in its outputs for every – clock input.

The carry out signal completes a full cycle for every 10/8-clock inputs cycle and is used as a ripple carry signal to any succeeding stages

Supply voltage range	3v to 15v
Noise immunity	0.45. V_{DD} typ:
TTL compatibility	Fanout of 2 driving 74L or 1 driving 74LS

Speed of operation = 0.5MHz typ. With $10V_{DD}$

Power 10μW typ

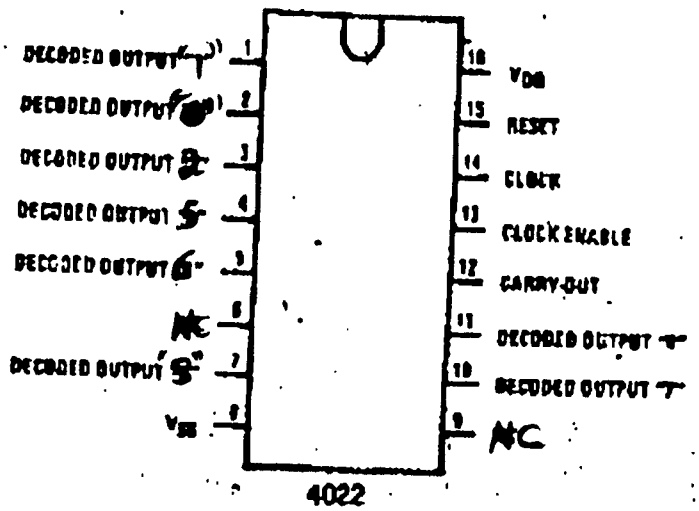


Fig 2.63A: THE CIRCUIT DIAGRAM OF THE 4022 DIVIDE BY 8 COUNTERED

	A	B	C	D	E	F	G	H
1	1	0	0	0	0	0	0	0
2	0	1	0	0	0	0	0	0
3	0	0	1	0	0	0	0	0
4	0	0	0	1	0	0	0	0
5	0	0	0	0	1	0	0	0
6	0	0	0	0	0	1	0	0
7	0	0	0	0	0	0	1	0
8	0	0	0	0	0	0	0	1

FIG 2.63B THE TRUTH TABLE DEFINING THE DIVIDE BY COUNTER/DIVIDER

2.3 THE CONTROLLER UNIT

The controller unit comprises the Hot Register, Delay and the Display Register. When the hot button is on, logic 0 is sent through the inverter and D input of the D – type flip flop of the hot register becomes logic 1. S_1 pulse passes through the enabled two – input AND gate to store the D input at Q.

Q at logic 1, completely enable the three (3) input AND gate in which S_2 is connected. A code from the counter is randomly latched into the 4 - 16 decoder.

S_3 is used to delay the display for about 3 seconds by using 4022B and the gated S_3 pulse, serving as the clock, completely enabled by the Q output from the Hot register. The delay is the total time taken for logic 1 to stop shift from decoded output 0 to 7 of the stepper/divider.

When decoded output 7 becomes logic 1, ad connected to the input of the display register, ungated S_4 clocks to store the logic at Q.

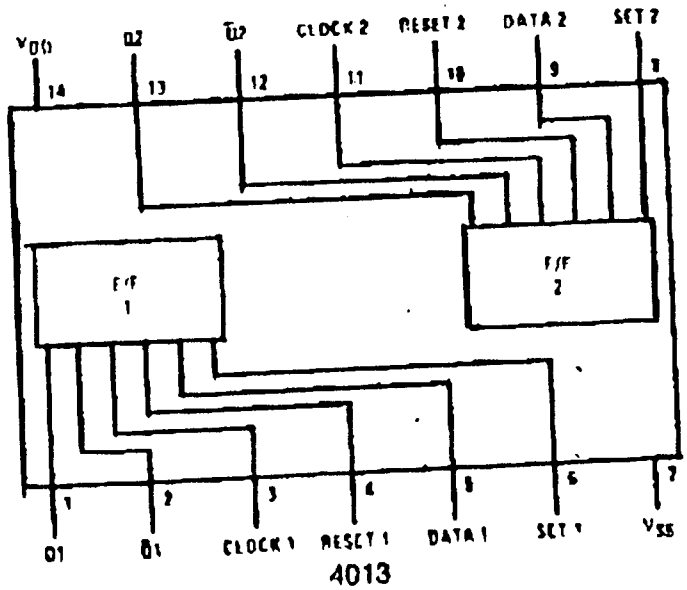
The logic state at Q is then used to activate the display unit as the display two (2) input AND gates are enabled by the state and the output of the YES – NO logic selector unit as well as the 4060B ripple carry counter signal.

2.71 THE HOT REGISTER

The Hot register is mainly made up of the 4013 BM dual D flip – flop. The 4013 device is a monolithic complementary MOS (CMOS) integrated circuit constructed with N – channel and P – channel enhancement transistors. Each flip – flop has independent data, set, reset clock inputs, Q and $\bar{Q}$ outputs. That can be used for shift register applications, and by connecting $\bar{Q}$ output to the data input, for counter and toggle application. The logic level present at the D input is transferred to the Q output during the positive – going transition of the clock pulse.

Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively. Whenever the Q output is high the $\bar{Q}$ output will be low and vise versa.

Supply voltage range	3v – 15v
Noise Immunity	$0.45V_{DD}$ typ
TTL Compatibility	fanout of 2 driving 74L or 1 driving 74LS



Truth Table
4013

CL1	D	R	S	Q	$\bar{Q}$
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	x	0	0	Q	$\bar{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

No change
↑ = Level change
x = Don't care case

Fig 2.71a

CIRCUIT DIAGRAM OF 4013 BM DUAL D FLIP FLOP

2.72 THE DISPLAY REGISTER

The display register is also made up of the same 4013BM DUAL D Flip flop as the Hot register in figure 2.71

2.73 THE DELAY/TIMER

The Delay/timer is mainly made up of the same 4022B stepper used for the selector in the YES – NO selector circuit unit in figure 2.63

2.8 THE YES COUNTER UNIT

The yes counter unit comprises three (3) of a digit seven segment display chips and three (3) of a digit 4026B decade. Whenever, yes code is accessed by the latch decoder, the unit is activated to count and display the number of YES picked while the seven segment display chips display the numbers in a digitalize form.

The counter unit is design to accommodate as much count as it could

2.81 THE DECADE COUNTER/ DIVIDER WITH DISPLAY ENABLE (4026B)

The decade counter/divider chip is made up of an in-built decade counter, binary coded decimal (BCD) decoder and seven (7) segment decoder/divider. The modulus of the decade counter is made to be 10 (That is, the counting sequence is made to be from 0000 to 1001 in binary codes which translates from 0 to 9 in decimal).

The modulus 10 counter has four place values; 8S, 4S, 2S and 1S. This takes four flip-flops connected as a ripple counter. A NAND gate is added to the ripple counter to clear all the flip- flops back to zero immediately after the 1001(9) count. This is achieved when the unit tires to advance to 1010 (10), the 2 highs (D=1, B=1) are fed into the NAND gate which activates and resets the display to 0000 as in figure 2.93.

The BCD decoder and the seven segment decoder serves as a BCD – to – seven segment decoder/driver. The basic function of a decoder is to detect the

presence of a specified output level. The BCD – to – seven segment decoder/driver. The basic function of a decoder is to detect the presence of a specified output level.

The BCD – to – seven-segment decoder/driver is a decoder that accepts the BCD code in its inputs and provides output to energize seven-segment display devices in order to produce a decimal readout.

The table below shows the desired truth table for common cathode seven-segment decoder/driver.

DISPLAY	D	C	B	A	A	B	C	D	E	F	G
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	1	0	0	0
8	1	0	0	0	1	1	1	0	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Table 2.81 TRUTH TABLE FOR BCD – TO – SEVEN SEGMENT DECODER/DRIVER (COMMON CATHODE).

From the expression in table 2.91, the logic for the BCD – to – seven-segment decoder can be implemented; that is, each of the ten BCD code words is decoded and then while decoding gates are ORed as dictated by the logic expression for each segment.

BCD – to – seven-segment decoder is also made up of two other inputs known as the BLANKING INPUT to clear the displays and a LAMP TEST to check the segment of the seven segment displays.

SEGMENT	USED IN DIGITS	LOGIC FUNCTIONS
A	0, 2, 3, 5, 6, 7, 8, 9.	$\bar{D}\bar{C}\bar{B}\bar{A}+\bar{D}\bar{C}\bar{B}A+\bar{D}C\bar{B}\bar{A}+\bar{D}CB\bar{A}+D\bar{C}\bar{B}\bar{A}+D\bar{C}\bar{B}A+D\bar{C}BA$
B	0, 1, 2, 3, 4, 7, 8, 9.	$\bar{D}\bar{C}B\bar{A}+\bar{D}\bar{C}BA+\bar{D}C\bar{B}\bar{A}+\bar{D}CB\bar{A}+\bar{D}CBA+D\bar{C}\bar{B}\bar{A}+D\bar{C}\bar{B}A.$
C	0, 1, 3, 4, 5, 6, 7, 8, 9	$\bar{D}\bar{C}B\bar{A}+\bar{D}\bar{C}BA+\bar{D}C\bar{B}\bar{A}+\bar{D}C\bar{B}A+\bar{D}CB\bar{A}+\bar{D}CBA+D\bar{C}\bar{B}\bar{A}+D\bar{C}\bar{B}A$
D	0, 2, 3, 5, 6, 8, 9	$\bar{D}\bar{C}\bar{B}\bar{A}+\bar{D}\bar{C}\bar{B}A+\bar{D}\bar{C}B\bar{A}+\bar{D}\bar{C}BA+\bar{D}C\bar{B}\bar{A}+\bar{D}CBA+D\bar{C}\bar{B}\bar{A}+D\bar{C}\bar{B}A.$
E	0, 2, 6, 8	$\bar{D}\bar{C}\bar{B}\bar{A}+\bar{D}\bar{C}B\bar{A}+\bar{D}C\bar{B}\bar{A}+\bar{D}CB\bar{A}.$
F	0, 4, 5, 6, 8, 9	$\bar{D}\bar{C}\bar{B}\bar{A}+\bar{D}\bar{C}B\bar{A}+\bar{D}C\bar{B}A+\bar{D}C\bar{B}\bar{A}+\bar{D}CB\bar{A}+D\bar{C}\bar{B}A$
G	2, 3, 4, 5, 6, 8, 9	$\bar{D}\bar{C}B\bar{A}+\bar{D}\bar{C}BA+\bar{D}C\bar{B}\bar{A}+\bar{D}C\bar{B}A+\bar{D}CB\bar{A}+D\bar{C}\bar{B}\bar{A}+D\bar{C}\bar{B}A.$

TABLE 2.82 SEVEN-SEGMENT DECODING FUNCTION LISTS WITH THE LOGIC FUNCTION FOR EACH OF THE SEGMENTS.

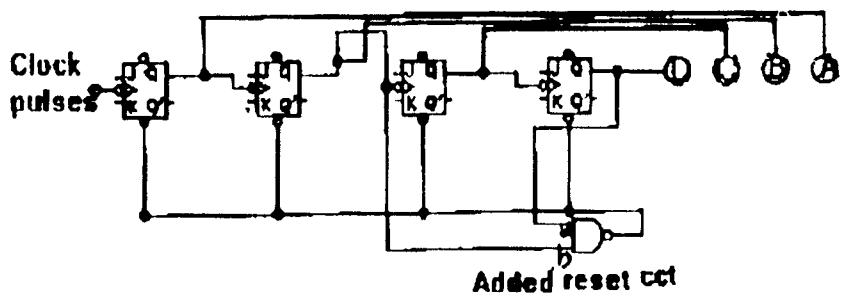


FIGURE 2.83 LOGIC DIAGRAM OF A MOD – 10 RIPPLE COUNTER

2.82 THE – SEVEN – SEGMENT DISPLAY

The common type of seven – segment display consist of light emitting diodes (LEDs) arranged as shown in figure 2.94. Each segment is a LED that emits light when current flows through it.

There are two types of arrangement:

- The common cathode and
- The common anode

Figure 2.84 is in common – cathode arrangement as used in the project design. Thus, it requires the drive to produce a HIGH level voltage to activate a segment. When a HIGH is applied to a segment input, the LED is forward biased and current flows through it.

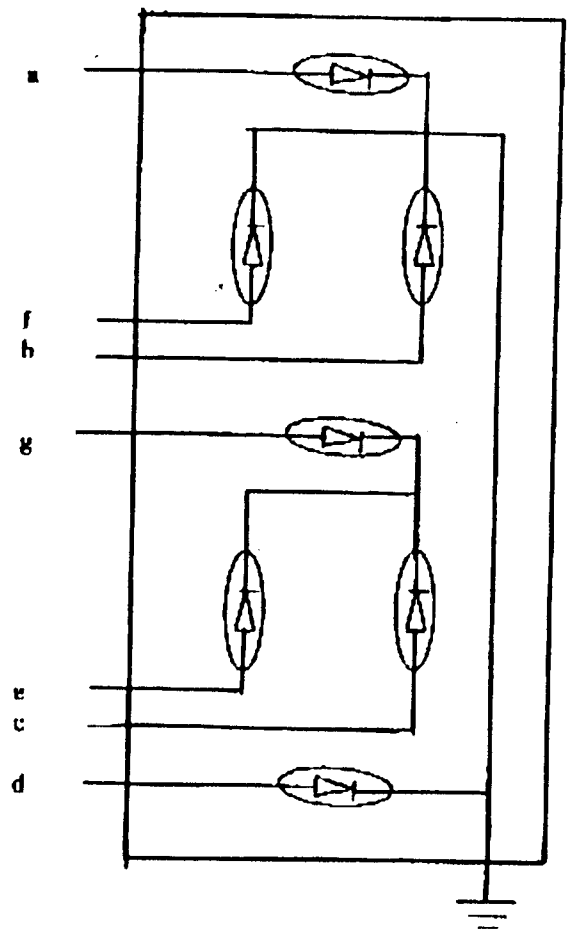


FIGURE 2.84: common cathode arrangement of seven – segment led displays

TABLE 2.83 Below lists the activated segments for each of the decimal digit.

DIGIT	SEGMENTS ACTIVATED
0	a, b, c, d, e, f
1	b, c
2	a, b, d, e, g
3	a, b, c, d, g
4	b, c, f, g
5	a, c, d, e, f, g
6	a, c, d, e, f, g
7	a, b, c
8	a, b, c, d, e, f, g
9	a, b, c, d, f, g

TABLE 2.83 shows the activated segments for each of the Decimal Digits.

FIGURE 2.85 shows the readout on seven-segment display of the decimal digits.

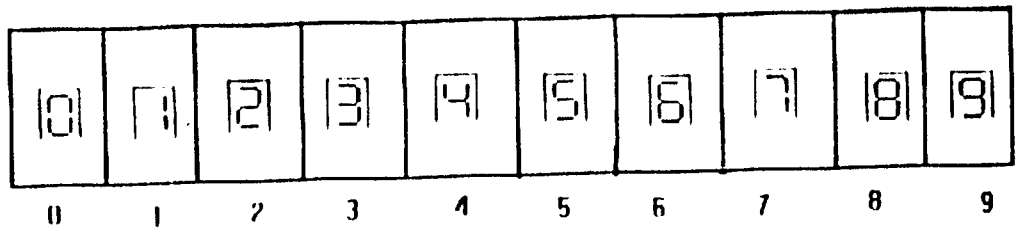


Fig 2.85 FORMAT OF READ OUTS ON SEVEN SEGMENT DISPLAY

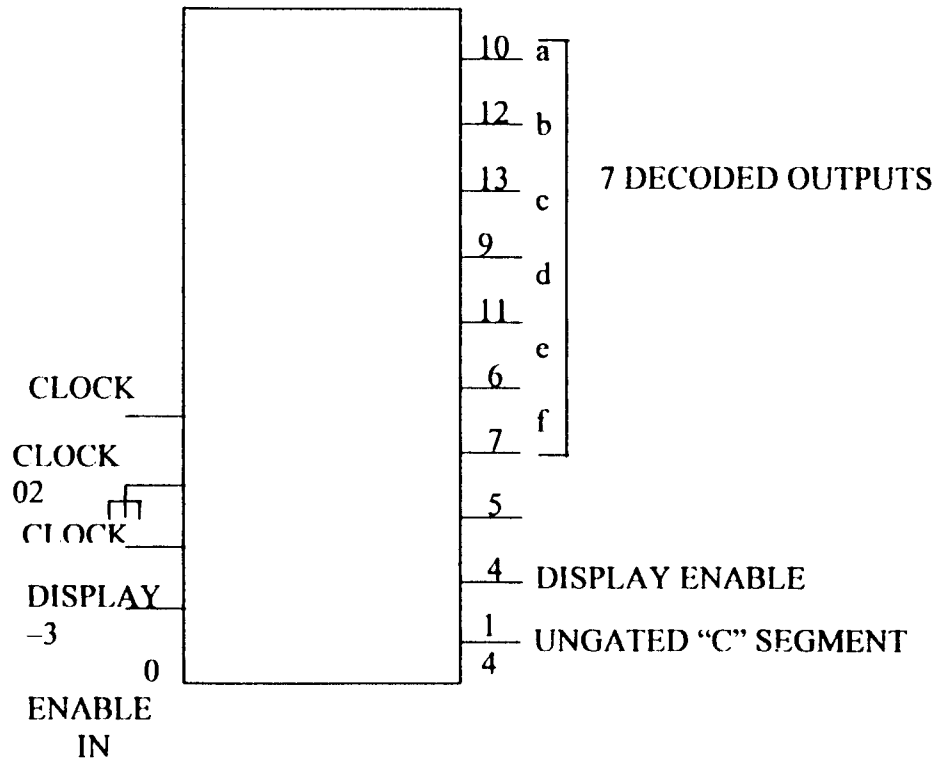
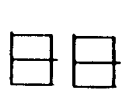


FIGURE 2.86 THE CIRCUIT DIAGRAM OF A DECADE COUNTER/DRIVER WITH DISPLAY ENABLE (4026B)

2.4 THE YES/NO DISPLAY UNIT

The YES/NO Display unit consists of a simple Resistor – Transistor (PNP) logic ROM and Resistors – Transistors (NPN) logic connected to the Light Emitting Diodes (LEDs) as a switch.

For the ROM, the Emitters of the PNP transistors are connected to the positive V_{cc} supply while the collectors are connected to the positive of its six (6) LEDs and the negative of the LEDs are grounded.

The Resistor – Transistors (NPN) logic connected as switches is in such a way that the Emitters are grounded while the collectors are connected to the negative of the LEDs and the positive of the LEDs are connected to the V_{cc}. That is, to say that the switches are connected in common collectors mode, so that each switch displays Y 

As said earlier, the simple ROM consists of to LED 1, 2, 3, 4, 5, and 6. The six are important for right display; That is, to display "yes" LEDs 1, 2 and 5 are responsible, while LEDs 3, 4 and 6 display "no".

Moreover, "Y" is controlled by the display driver, logic 1 from the output of the circuit switches on "Y" while logic 0 does otherwise; that is no.

The blinking effect of the Display is accomplished by gating the cathode with an 8Hz pulse. The cathode current flows after the display register has been activated, while all the LEDs without 1, 2, 3, 4, 5 and 6 are "on" and the display ROM switches specific LEDs to form the corresponding word, "yes" or "no". The six transistors are grouped into two so that three are responsible for each display.

CHAPTER THREE

CONSTRUCTION AND TESTING

3.1 INTEGRATED CIRCUIT AND CHOICE OF LOGIC FAMILY

An integrated circuit is a complete electronic circuit containing active and passive components fabricated of an extremely tiny single chip of silicon. With the introduction of ICs, designer job has been made easier by replacing individual components designed in a complete circuit diagram with just a single IC chip.

Such has helped greatly in this project too, by replacing almost all of the components in a module ICs such as latch decoder, decade counter/driver with display enable, seven – segment display e.t.c.

There are variety of technologies for fabricating electronic gates I integrated circuits. The logic family to employ depends largely on speed, power consumption, number of circuits per unit chip area and application. A logic (DIGITAL) family is a group of compatible devices with the same logic levels and supply voltages. So, after designing a device or system, it is important to know which logic family to choose during construction.

Logic circuits of any complexity are interconnections of basic logic gate circuits specified by the following:

i. Small – scale integration (SSI).

ii. Medium – scale integration (MSI).

iii. Large – scale integration (LSI)

ii. very large scale integration (VLSI)

ICs in a family are said to be compatible and they can be easily connected. IC's of different families can also be interfaced. There are two major families of IC's and digital electronics.

They are:

a. BIPOLAR TECHNOLOGY: These ICs contain bipolar transistors, diodes and resistors

b. METAL OXIDE SEMICONDUCTOR (MOS)

A. BIPOLAR sub families are:

1. Resistor – Transistor Logic (RTL)

2. Diode – Transistor Logic (DTL)

3. Transistor – Transistor Logic (TTL)

4. Emitter – coupled Logic (ECL)

B. MOS sub families are:

1. P – channel metal oxide semi – conductor (PMOS)

2. N – channel metal oxide semi – conductor (NMOS)

3. Complementary metal oxide semi – conductor (CMOS)

The TTL and CMOS technology are commonly used to fabricate SSI and MSI integrated circuits for functional devices such as logic gates, flip – flops, encoder e.t.c.

For the purpose of this project work, the B series from the CMOS family was used because of its extended supply voltage range and its compatibility with RTL.

The RTL technology was used for its ruggedness, low power consumption, easy to handle, and its availability.

3.2 HARDWARE CONSTRUCTION

In the hardware construction of the system, the overall system was broken into eight modules for easy construction, testing and trouble shooting.

i. Power supply unit

ii. Oscillator unit

iii. Counter unit

iv. Latch/ 4 – 16 decoder unit

v. Yes – no logic selector circuit unit

vi. Controller unit

vii. Yes counter unit

viii. Yes/No display unit

MODULE 1: Power Supply Unit

The module was built with transformer as the first component on the veroboard. The primary end of the transformer was connected to AC card with AC indicator. The secondary winding was connected to two legs of the bridge rectifier marked AC. Across the two other legs of the rectifier is electrolytic capacitor connected with the right polarity. The positive and negative output of the capacitor were fed to Pin 1 and 2 respectively of the 3 – leg regulator IC with Pin 3 as the output.

A LED indicator with limiting resistor was connected across the output of the 9V output of the regulator to serve as indicator with the polarities of the LED taken into consideration.

MODULE 2: Oscillator Unit

This module houses the 14 – stage Ripple Carry binary counter (4060) with an inbuilt RC oscillator and a divider that divides its generated waveform into 10 different oscillatory frequencies corresponding to the RC oscillatory frequency of about 1KHz generated to oscillate the four input – 16 – codes counter, the mini controller section and the display unit.

Three of the Q outputs of the 4060B counter of different square wave frequency level were connected to the clocks of the latch/4 – to – 16 line decoder, divide by 8 counter/driver of the mini controller sub section and the AND gate of the display unit with P in legs of the 4060B, 4022B, 4520B ICs taking into consideration.

MODULE 3: Counter Unit

This module involve the feeding of the four (4) Q outputs of one of the two identical, independent, synchronous 4 – stage of the dual synchronous up counter via connections as input to the four bit latch/4 – to – 16 line decoder while mounted on the veroboard, as their Pin legs being considered from the manufacturer data sheet. The remaining unused Pin legs in the module were grounded.

MODULE 4: Latch/ 4 – 16 decoder unit

This module involve the connections of some of the latch decoder outputs to the inputs of the Yes – no – logic selector circuit unit OR gates while the output of each gate and three of the divide by 8 counter/divider decoded outputs of the selector circuit, that is, one or each were fed as input to the selector circuit AND gates via connections, so that one of the gates could be selected at a time to activate the three input OR gate whenever a yes code is accessed.

MODULE 5: Yes – no logic selector circuit unit.

In this module, the output of the selector circuit AND gates were connected to an OR gate while the output of the same gate was fed with the connection from the delay Pin of the controller sub unit 4022B(stepper) and the Q output of display register D flip – flop as input to the three input AND gate mounted to clock the yes counter unit.

The output of the selector circuit three input OR gate with the output of the ANDed Q output of the display register D flip – flop and one of the output Pin(d) of the 4060B Counter were gated to the Y display Resistor – Transistor logic switch to aid in the display and blinking action of Y whenever the output of the three input OR fate is high.

The (d) output was also fed to the "es/no" Resistor – Transistor logic switch for their display and blinking action, while output A was inverted via 4069B inverter and fed to three of the Resistor – Transistor logic of the ROM

MODULE 7: Yes counter unit

The connections in this module involve the feeding of the ANDed output (c) from the Yes – no logic selector circuit unit to the clock pin out of one of the 34026B Decade counter/driver while their reset Pin outs were connected to the inverted input voltage (V_{cc}).

The seven decoded outputs of the three counters Pin outs were also connected to the input Pin outs of the three seven segment display meant for each counter for their digitalized counting from 000 to 999.

MODULE 8: Yes/No display unit.

This module houses the ANDed output A from the Yes – no logic selector circuit unit and the ANDed output of **a** with the Q output of the display register D flip – flop (d) to the Y Resistor – Transistor logic switch and the d pin out to the Resistor – Transistor logic switch for SO and en displays as well as the display ROM.

The Rom consist of six (6) transistors with their output stages connected to LED 1, 2, 3, 4, 5, and 6 as shown in the circuit diagram of the entire project.

3.3 COMPONENT LAYOUT

The followings were observed and done while constructing the hardware:

1. Almost all of the ICs were mounted on IC sockets already soldered to the veroboard to ease replacement of any faulty or bad IC in future.

2. Interconnections were made through etching of the veroboard and the use of insulated copper wire connected at the bottom of the verobound while the components were mounted on the top of the verobound and soldered underneath thus giving the components good layout and space to give room for ventilation, trouble shooting and replacement of faulty components.

3. All ICs were laid is in such a way that they point to the same direction. This makes it easier to keep track of pin numbers during connection and easy replacement in case of any damage to the IC in question.

4. The leads or legs of various components such as capacitors, resistors, leds and so on were reduced so as to prevent short circuit.

5. Finally, the system was carefully laid out and planned in such a way to simplify wiring, minimize error and make trouble shooting easier.

3.4 PACKAGING AND BOXING

The constructed hardware was caged in a box made of wooden frames. The base and sides of the box contains the hardware components of the system. system. Fig 3.4 below gives a detailed diagram about the positions of the mounted components and modules as well as materials used for the construction of the box.

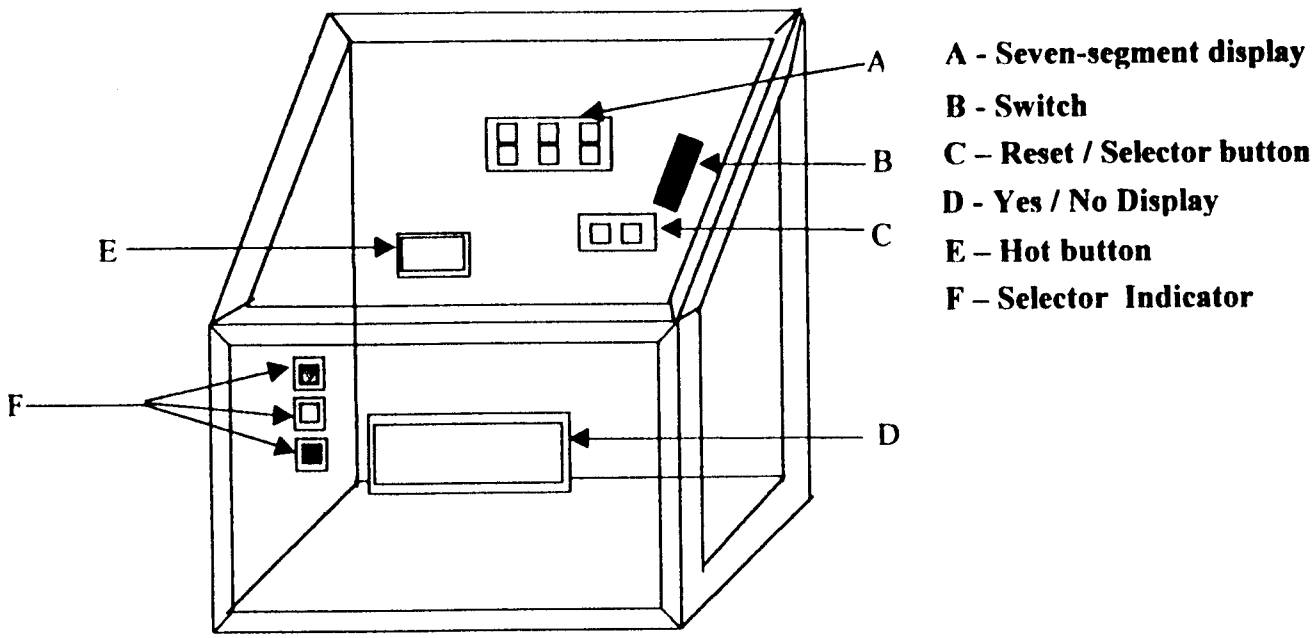


Fig.3.4: Detailed diagram of the casing.

3.5 CONSTRUCTION TOOLS USED

Most of the construction tools used during modeling and hardware construction are given below;

a. veroboard and insulated copper wire: This is where the prototype model was permanently mounted

b. Soldering Iron and lead: A 40W Soldering Iron and lead were used in soldering all components together on board.

c. Veroboard and coated copper wire: This was where the final circuit was permanently mounted and soldered with coated copper wire used for routing and conducting currents and signals from one components to another.

d. Wire cutter, Blade and Pliers: these were used in cutting wires to appropriate length and preparing the insulated ends of the wires for soldering.

e. Fine file, wet and emery cloth: They are used to prepare the tips of the soldering bit and to desolder smudges from the surface of the solder bit.

f. Digital Multimeter : This device was used to test the continuity of line and to measure voltages, currents and resistance outputs of the components in the circuit during construction.

g. Sunction Tube: this was used to suck desoldered lead away from unwanted area.

3.6 HARDWARE TESTING

At the end of the hardware construction, a careful hardware test of the completed circuit was carried out as follows:

STEP 1:

Continuities of copper wires used in the construction were tested using a multimeter.

STEP 2:

Multimeter was also used to ascertain that there was no short between the power supply and ground.

STEP 3:

The polarities of components were tested and checked by same testing tool above.

STEP 4:

ICs were checked to reaffirm their correct placement in IC sockets.

STEP 5:

The output voltage of the transformer used was observed and measured to be 12 volts as expected.

STEP 6:

The output IC voltage regulator was measured to be 9V as produced by 7809 IC regulator.

STEP 7:

The switches, reset and hot buttons were tested and certified OK.

STEP 8:

The overall operation of the circuit was tested with overall effect of count initiation and the display at the Yes/no display unit.

3.7 TESTING TOOL USED

The only testing tool used during hardware test of the system is the multimeter; The device was used to test the continuity of lines and to measure voltage, current and resistance of an output, component and modules of the entire system.

3.8 OPERATION

As the set button is pressed the oscillator triggers the counter and operates the control section or panel which results into a cycle oscillation of 16 binary codes. The memory latch and allow the switch to access just one binary

code from the counter to memory during the rapid cycle and code is linked to the latch decoder which allow one of its output corresponding to the input to be logic one in order foe a signal to be sent to the display the option that was access after passing through the yes/no selector circuit unit. The reset button is used to reset the system as well as clearing the display unit for the next person to ballot.

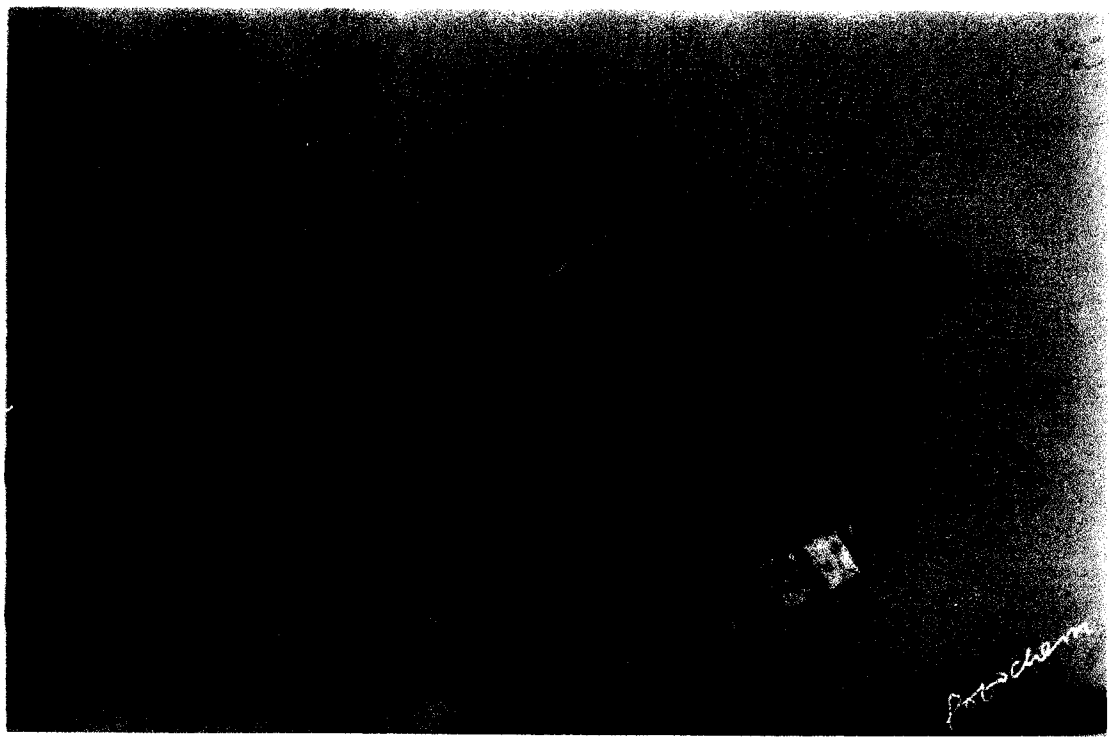


FIG. 3.1 THE PHOTOGRAPH OF THE COMPLETE CIRCUIT OF THE DIGITAL ELECTRONIC BALLOT MACHINE.

CHAPTER FOUR

DISCUSSION, CONCLUSION AND RECOMMENDATION

4.1 DISCUSSION OF RESULT

As seen from the hardware test carried out, the device always work on the principle of set, execute and reset mode at a time required to be used in a particular environment. The device also uses one voltage source of nine volts throughout its entire system. The 4060B serve as the initiator or foundation for the execution process of the system, while the display and the yes-counter unit serve as the revealer of what was being executed by the ballot machine.

4.2 CONCLUSION

In conclusion, the motive and objective of this designs, that is, to modernize or introduce automation into ballot process have been realised as observed from the hardware testing and operation thus proving further that DIGITAL ELECTRONIC BALLOT MACHINE can be constructed from the basic principle of digital, integrated circuit components at a cheaper rate.

4.3 RECOMMENDATION

My desire as an electrical and computer engineer is to fully automate the ballot activities in our institutions of higher learning, thus facilitating the ease of hostel accommodation ballot and counting evaluation of figures.

The design and construction of this ***Digital Electronic Ballot Machine*** is the beginning of an automation and computerization era in the higher learning institutions ballot activities.

Meanwhile, this work should serve as an eye opener to whoever might be interested in the computerization of the ballot process.

I hereby recommend this design for use in Nigeria institutions of higher learning.

For future recommendation on this system the following guidelines should be observed:

1. A sound unit could be initiated to the system via the yes – no logic selector unit output, so that yes can also be recognize by sound.
2. The display unit could be made in form of a liquid crystal display, which consume less power.
3. The yes - no logic selector circuit could be reprogrammed to increase the number of yes to 32, 16 and 8 according to the accommodation available to the students.

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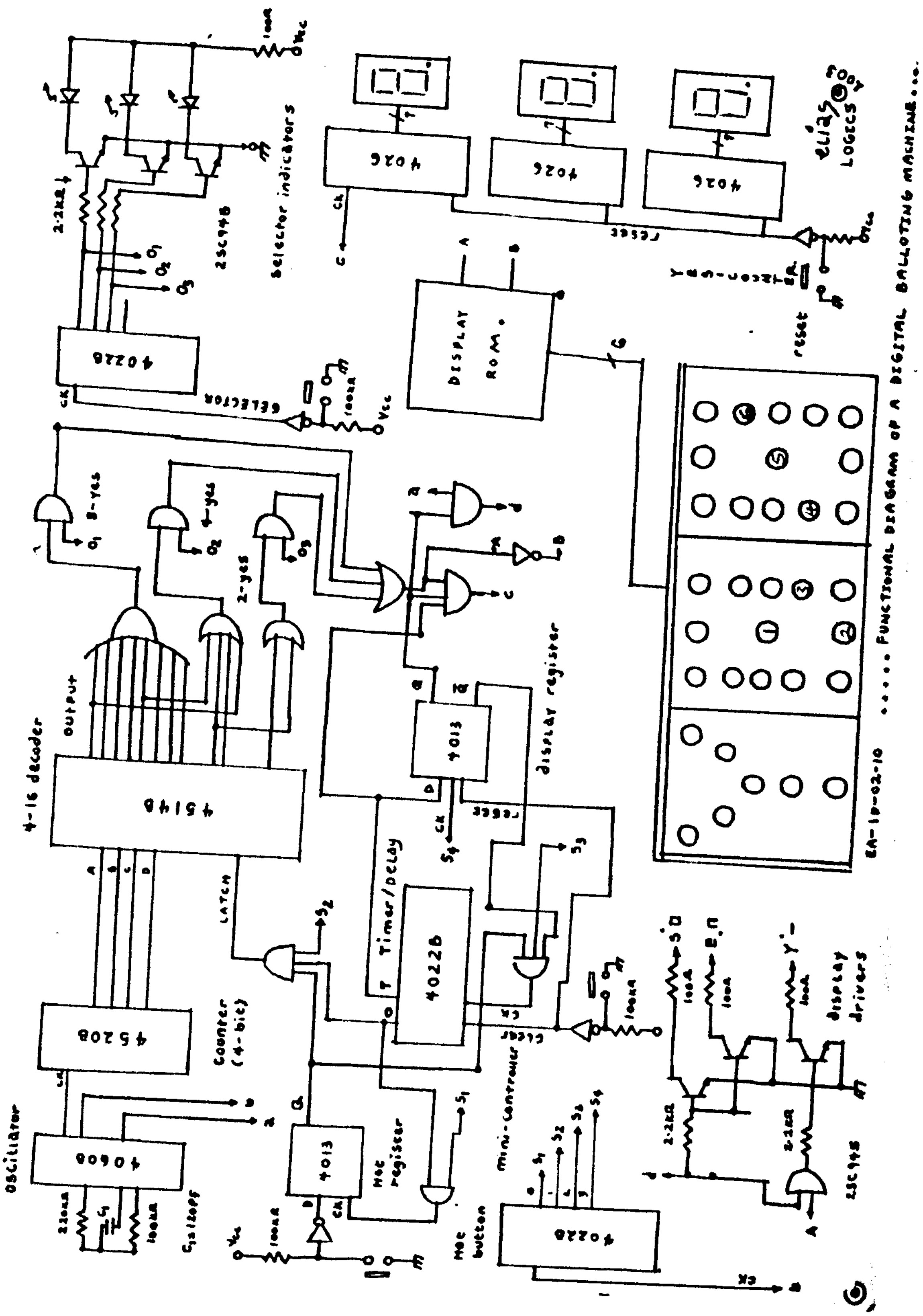
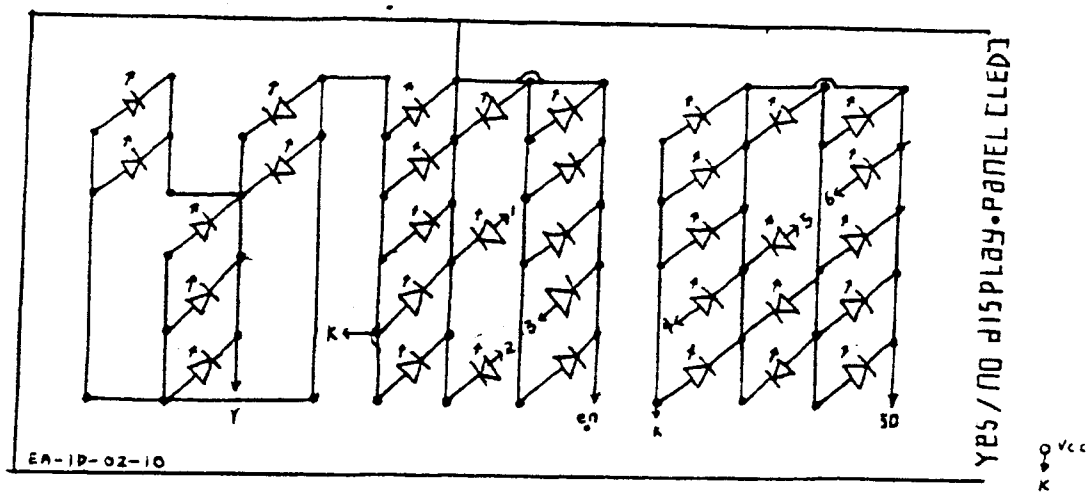
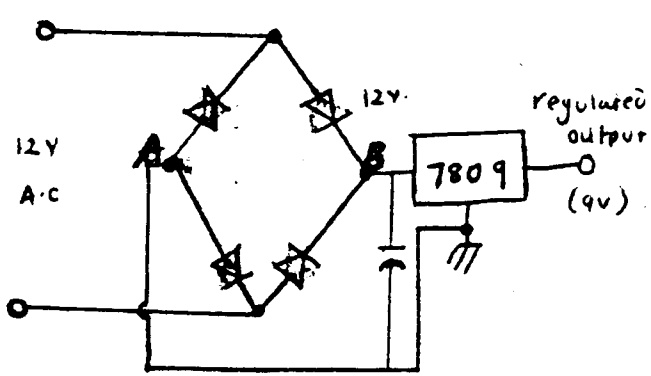
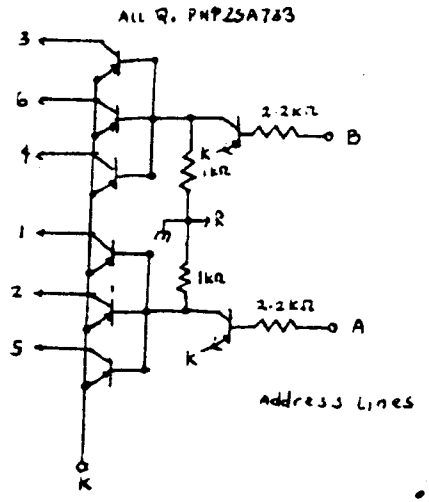


..... FUNCTIONAL DIAGRAM OF A DIGITAL BALLOTING MACHINE....
Elias Logics
EA-19-02-10
Oscillator
40608
Counter (4-bit)
45208
4-16 decoder
45148
Output
LATCH
8-yes
4-yes
2-yes
Selector indicators
2SC945
40228
SELECTOR
DISPLAY ROM.
4026
reset
Timer/Delay
40228
4013
display register
Mic register
Mic button
mini-controller
40228
display drivers
CLEAR







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